Siliconix

VMOS Power FETs Design Catalog

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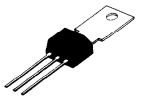
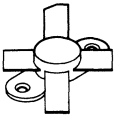
SEMICONDUCTOR DEVICES

VMOS Device/Application Selector

LOGIC SWITCHING • Computer Interface • Telephone Muting Switch, Central Office Equipment, PABX Equipment • Microprocessor Systems • Data Acquisition Systems • Computer Peripheral Equipment • Industrial Process Controls • Relay Replacement/Driver	2N6659 S55V01 S55V12 VN46AF	2N6660 S55V02 S55V21 VN66AF	2N6661 S55V11 S55V22 VN88AF
HIGH SPEED SWITCHING • Optical Data Transmission • Bubble Memory Driver • R-R Relay Replacement • Laser Diode Pulsing • Instruments	VMP4 VN98AJ VN98AK	VN33AJ VN33AK	VN66AJ VN66AK
POWER SWITCHING • DC/DC Converters • DC/AC Inverters • OEM & Main Frame Power Supplies • Motor Controllers	2N6656 2N6659 VN46AF	2N6657 2N6660 VN66AF	2N6658 2N6661 VN88AF
BRIDGE SWITCHING • 3 ϕ Power Supplies • Motor Controllers	VN33AJ VN33AK	VN66AJ VN66AK	VN98AJ VN98AK
R-F AMPLIFIERS • Communications • EW & ECM • Microwave Transmission in Telecom • Mobile	VMP4 VN98AJ VN98AK	VN33AJ VN33AK	VN66AJ VN66AK
SERVO	2N6656 VN46AF	2N6657 VN66AF	2N6658 VN88AF
AUDIO • Consumer Audiophile	2N6656 VN46AF	2N6657 VN66AF	2N6658 VN88AF

VMOS Selector Guide

SATURATED ON VOLTAGE ($V_{DS(ON)}$ @ I_D = 1 AMP, V_{GS} = 10 V) (VOLTS)	BREAKDOWN VOLTAGE (BV_{DSS} @ I_D = 10 μA)						PACKAGE
	90 V		60 V		35 V		
	ZENER	NON-ZENER	ZENER	NON-ZENER	ZENER	NON-ZENER	
4.5	S55V12	VN99AJ					
4.0	2N6658	VN98AJ					
3.5			S55V01	VN67AJ			
3.0			2N6657	VN66AJ			
2.5					S55V11	VN35AJ	
1.8					2N6656	VN33AJ	TO-3
4.5	S55V22	VN99AK					
4.0	2N6661	VN98AK					
3.5			S55V02	VN67AK			
3.0			2N6600	VN66AK			
2.5					S55V21	VN35AK	
1.8					2N6659	VN33AK	TO-39
	80 V		60 V		40 V		
4.0	VN88AF						
3.0			VN66AF		VN46AF		
							TO-202
3.0				VMP4			
							380-SOE

n-channel enhancement-mode VMOS Power FETs *designed for . . .*

- **High Speed Switching**
- **CMOS to High Current Interface**
- **TTL to High Current Interface**
- **High Frequency Linear Amplifiers**
- **Line Drivers**
- **DC to DC Converters**
- **Switching Power Supplies**

Performance Curves VNAZ
See Section 3

BENEFITS

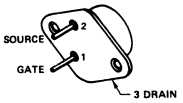
- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
  - Low Drive Current (I_{GSS} < 100 nA)
  - Threshold Voltage 0.8 to 2.0 V
- Permits More Efficient and Compact Switching Designs
  - Typical T_{ON} and T_{OFF} < 5 nsec
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From a CMOS Logic Gate > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

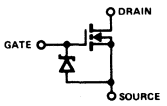
ABSOLUTE MAXIMUM RATINGS

*Maximum Drain-Source Voltage	
2N6656	35 V
2N6657	60 V
2N6658	90 V
*Maximum Drain-Gate Voltage	
2N6656	35 V
2N6657	60 V
2N6658	90 V
*Maximum Continuous Drain Current	2.0 A
Maximum Pulsed Drain Current	3.0 A
*Maximum Continuous Forward Gate Current	2.0 mA
*Maximum Pulsed Forward Gate Current	100 mA
*Maximum Continuous Reverse Gate Current	100 mA
*Maximum Forward Gate-Source (Zener) Voltage	15 V
*Maximum Reverse Gate-Source Voltage	0.3 V
*Maximum Dissipation at 25°C Case Temperature	25 W
*Linear Derating Factor	200 mW/°C
*Temperature (Operating and Storage)	−55 to +150°C
*Lead Temperature (1/16" from case for 10 sec)	300°C

*Indicates JEDEC registered data

TO-3
See Section 4





ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

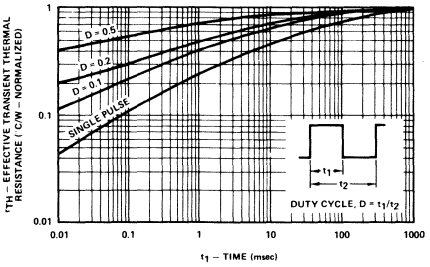
		Characteristic	2N6656 Min	2N6656 Typ	2N6656 Max	2N6657 Min	2N6657 Typ	2N6657 Max	2N6658 Min	2N6658 Typ	2N6658 Max	Unit	Test Conditions
1		BV_{DSS} Drain-Source Breakdown	35			60			90			V	V_{GS} = 0, I_D = 10 μA
2			35			60			90				V_{GS} = 0, I_D = 2.5 mA
3*		$V_{GS(th)}$ Gate Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1 mA
4*		I_{GSS} Gate-Body Leakage		0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15 V, V_{DS} = 0
5*					500			500			500		V_{GS} = 15 V, V_{DS} = 0, T_A = 125 °C (Note 2)
6*		I_{DSS} Zero Gate Voltage Drain Current			10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0
7*	STATIC				500			500			500		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125 °C (Note 2)
8				100			100			100		nA	V_{DS} = 25 V, V_{GS} = 0
9*		$I_{D(on)}$ ON-State Drain Current (Note 1)	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25 V, V_{GS} = 10 V
10		$V_{DS(on)}$ Drain-Source Saturation Voltage (Note 1)		0.3			0.3			0.4		V	V_{GS} = 5 V, I_D = 0.1 Amp
11				1.0	1.5		1.0	1.5		1.1	1.6		V_{GS} = 5V, I_D = 0.3 Amp
12				0.9			0.9			1.3			V_{GS} = 10 V, I_D = 0.5 Amp
13*				1.6	1.8		2.0	3.0		3.0	4.0		V_{GS} = 10 V, I_D = 1.0 Amp
14		$r_{DS(on)}$ Static Drain-Source ON-State Resistance		1.6	1.8		2.0	3.0		3.0	4.0	Ω	V_{GS} = 10 V, I_D = 1.0 Amp
15*		$r_{ds(on)}$ Small-Signal Drain-Source ON-State Resistance		1.6	1.8		2.0	3.0		3.0	4.0		V_{GS} = 10 V, I_D = 0, f = 1 kHz
16		g_{fs} Forward Transconductance (Note 1)	170	250		170	250		170	250		mΩ	V_{DS} = 24 V, I_D = 0.5 Amp
17*		C_{iss} Input Capacitance (Note 2)			50			50			50	pF	V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz
18*	DYNAMIC	C_{ds} Drain-Source Capacitance (Note 2)			40			40			40		
19		C_{rss} Reverse Transfer Capacitance (Note 2)			10			10			10		V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz
20*					35			35			35		V_{GS} = 0, V_{DS} = 0, f = 1.0 MHz
21*		$t_{d(on)}$ Turn-ON Delay Time (Note 2)		2	5		2	5		2	5	ns	See Switching Time Test Circuit VNAZ, Section 3
22*		t_r Rise Time (Note 2)		2	5		2	5		2	5		
23*		$t_{d(off)}$ Turn-OFF Delay Time (Note 2)		2	5		2	5		2	5		
24*		t_f Fall Time (Note 2)		2	5		2	5		2	5		

*Indicates JEDEC registered data

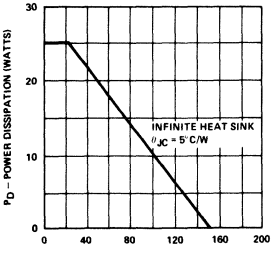
VNAZ

NOTES:
1. Pulse test—80 μsec pulse, 1% duty cycle.
2. Sample test.

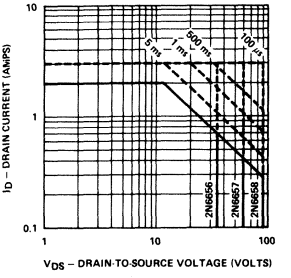
Thermal Response



Power Dissipation vs Case Temperature



Maximum Safe Operating Region



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

- **High Speed Switching**
- **CMOS to High Current Interface**
- **TTL to High Current Interface**
- **High Frequency Linear Amplifiers**
- **Line Drivers**
- **Switching Power Supplies**

Performance Curves VNAZ
See Section 3

BENEFITS

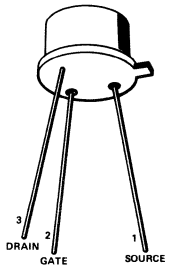
- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
  - Low Drive Current ($I_{GSS} < 100$ nA)
  - Threshold Voltage 0.8 to 2.0 V
- Permits More Efficient and Compact Switching Designs
  - Typical T_{ON} and $T_{OFF} < 5$ nsec
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From a CMOS Logic Gate > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases as Temperature Increases
  - Input Protected from Static Discharge

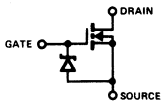
ABSOLUTE MAXIMUM RATINGS

*Maximum Drain-Source Voltage	
2N6659	35 V
2N6660	60 V
2N6661	90 V
*Maximum Drain-Gate Voltage	
2N6659	35 V
2N6660	60 V
2N6661	90 V
*Maximum Continuous Drain Current	2.0 A
Maximum Pulsed Drain Current	3.0 A
*Maximum Continuous Forward Gate Current	2.0 mA
*Maximum Pulsed Forward Gate Current	100 mA
*Maximum Continuous Reverse Gate Current	100 mA
*Maximum Forward Gate-Source (Zener) Voltage	15 V
*Maximum Reverse Gate-Source Voltage	0.3 V
*Maximum Dissipation at 25°C Case Temperature	6.25 W
*Linear Derating Factor	50 mW/°C
*Temperature (Operating and Storage)	−55 to +150°C
*Lead Temperature (1/16" from case for 10 seconds)	300°C

*Indicates JEDEC registered data

TO-39
See Section 4





*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		2N6659			2N6660			2N6661			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	BV_{DSS}	Drain-Source Breakdown	35			60			90			V	V_{GS} = 0, I_D = 10 μA
2				35			60			90				V_{GS} = 0, I_D = 2.5 mA
3*		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1 mA
4*		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15 V, V_{DS} = 0
5*						500			500			500		V_{GS} = 15 V, V_{DS} = 0, T_A = 125°C (Note 2)
6*		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0
7*						500			500			500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)
8					100			100			100		nA	V_{DS} = 25 V, V_{GS} = 0
9*		$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25 V, V_{GS} = 10 V
10		$V_{DS(on)}$	Drain-Source Saturation Voltage (Note 1)		0.3			0.3			0.4		V	V_{GS} = 5 V, I_D = 0.1 Amp
11					1.0	1.5		1.0	1.5		1.1	1.6		V_{GS} = 5 V, I_D = 0.3 Amp
12					0.9			0.9			1.3			V_{GS} = 10 V, I_D = 0.5 Amp
13*					1.6	1.8		2.0	3.0		3.0	4.0		V_{GS} = 10 V, I_D = 1.0 Amp
14*		$r_{DS(on)}$	Static Drain-Source ON-State Resistance (Note 1)		1.6	1.8		2.0	3.0		3.0	4.0	Ω	V_{GS} = 10 V, I_D = 1.0 Amp
15*		$r_{ds(on)}$	Small-Signal Drain-Source ON-State Resistance		1.6	1.8		2.0	3.0		3.0	4.0		V_{GS} = 10 V, I_D = 0, f = 1 kHz
16		g_{fs}	Forward Transconductance (Note 1)	170	250		170	250		170	250		m℧	V_{DS} = 24 V, I_D = 0.5 Amp
17*	DYNAMIC	C_{iss}	Input Capacitance (Note 2)			50			50			50	pF	V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz
18*		C_{ds}	Drain-Source Capacitance (Note 2)			40			40			40		
19		C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10		V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz
20*						35			35			35		V_{GS} = 0, V_{DS} = 0, f = 1.0 MHz
21*		$t_{d(on)}$	Turn-ON Delay Time (Note 2)		2	5		2	5		2	5	ns	See Switching Time Test Circuit VNAZ, Section 3
22*		t_r	Rise Time (Note 2)		2	5		2	5		2	5		
23*		$t_{d(off)}$	Turn-OFF Delay Time (Note 2)		2	5		2	5		2	5		
24*		t_f	Fall Time (Note 2)		2	5		2	5		2	5		

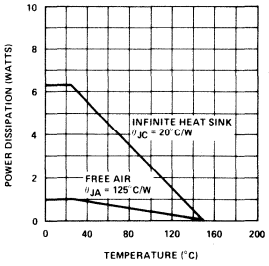
*Indicates JEDEC registered data

VNAZ

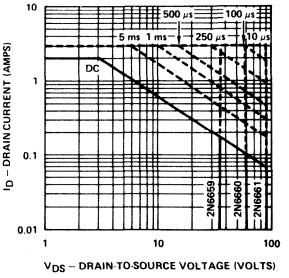
NOTES:

1. Pulse test—80 μsec pulse, 1% duty cycle.
2. Sample test.

Power Dissipation vs Case or Ambient Temperature



Maximum Safe Operating Region



high speed, power peripheral drivers (2.0 A, 35-90 V) *designed for . . .*

- **Peripheral Drivers for EDP and Process Control Systems**
- **Laser Diode Pulsing**
- **High Speed Line Drivers**
- **CMOS to High Current Interfacing**
- **TTL to High Current Interfacing**
- **Switching Reactive Loads**

ABSOLUTE MAXIMUM RATINGS

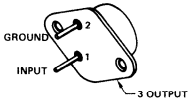
Output Voltage
- S55V11 . . . . . 35 V
- S55V01 . . . . . 60 V
- S55V12 . . . . . 90 V

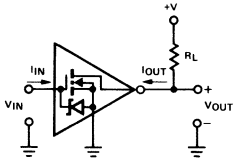
Continuous Output Current . . . . . 2.0 A
Peak Output Current . . . . . 3.0 A
Continuous Input Current . . . . . 2.0 mA
Peak Input Current . . . . . 100.0 mA
Voltage at Input . . . . . 15 V
Reverse Input Voltage . . . . . −0.3 V
Power Dissipation at 25°C Case Temperature . . . . . 25 W
Storage Temperature . . . . . −55°C to 150°C
Operating Temperature . . . . . −55°C to 150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
  - Low Drive Current (I_{GSS} < 100 nA)
  - Threshold Voltage 0.8 to 2.0 V
- Fan Out From CMOS > 100
- No Power Supply Connection Required
- Permits Improved Data Transmission Times
  - Propagation Delay Typically 4 nsec
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - High Gain > 10 Meg @ 1.0 Amp
  - High Speed
  - Free From Failure Due to Secondary Breakdown and Thermal Runaway
  - Paralleled Easily Without Current Sharing Resistors
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

TO-3
See Section 4

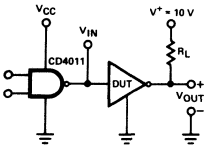




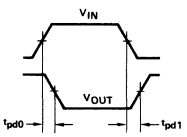
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

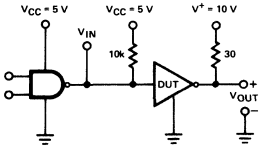
	Characteristic		S55V11			S55V01			S55V12			Unit	Test Conditions
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	V_{IN}	Logical "1" Input Voltage (Note 2)	4.0	2.0		4.0	2.0		4.0	2.0		V	I_O = 100 mA, V_{OUT} = 25 V
2			5.0	3.5		5.0	3.5		5.0	3.5			I_O = 300 mA, V_{OUT} = 25 V
3			10.0	6.5		10.0	6.5		10.0	6.5			I_O = 1 Amp, V_{OUT} = 25 V
4	V_{IN}	Logical "0" Input Voltage (Note 2)		1.2	0.8		1.2	0.8		1.2	0.8		I_O = 1.0 mA, V_{OUT} = 25 V
5				0.8			0.8			0.8			I_O = 0.1 mA, V_{OUT} = 25 V
6					0			0			0		I_O = 10 μA, V_{OUT} = 25 V
7	I_{IH}	Logical "1" Input Current		0.01	0.5		0.01	0.5		0.01	0.5	μA	V_{IN} = 10 V, V_{OUT} = 0
8	I_{IL}	Logical "0" Input Current (Note 2)		−0.01			−0.01			−0.01			V_{IN} = 0V, V_{OUT} = 25 V
9	V_{ON}	Output Breakdown Voltage	35			60			90			V	I_O = 10 μA, V_{IN} = 0
	Specifications For Use With CMOS (Figure 1)												
10	V_{OL}	Output ON Voltage (Note 1)		0.3			0.3			0.4		V	I_O = 100 mA, V_{IN} = 5 V
11				1.0	1.5		1.0	1.5		1.4	1.7		I_O = 300 mA, V_{IN} = 5 V
12				1.8	2.5		2.2	3.5		3.8	4.5		I_O = 1.0 Amp, V_{IN} = 10 V
13	t_{pd0}	Propagation Delay to Logical "0" Output (Note 2)		4	10		4	10		4	10	ns	Figure 1, R_L = 10 Ω, V_{CC} = 10 V
14				5			5			5			Figure 1, R_L = 30 Ω, V_{CC} = 5 V
15	t_{pd1}	Propagation Delay to Logical "1" Output (Note 2)		4	10		4	10		4	10		Figure 1, R_L = 10 Ω, V_{CC} = 10 V
16				5			5			5			Figure 1, R_L = 30 Ω, V_{CC} = 5 V
	Specifications For Use With TTL (Figure 2)												
17	V_{OL}	Output ON Voltage (Note 1)		0.3			0.3			0.4		V	I_O = 100 mA, V_{IN} = 5 V
18				1.0	1.5		1.0	1.5		1.4	1.7		I_O = 300 mA, V_{IN} = 5 V
19	t_{pd0}	Propagation Delay to Logical "0" Output (Note 2)		8			8			8		ns	Figure 2
20	t_{pd1}	Propagation Delay to Logical "1" Output (Note 2)		5			5			5			Figure 2

NOTES:
1. Pulse Test – 80 μs pulse, 1% duty cycle.
2. Sample Test



CMOS Switching Circuit
Figure 1





TTL Switching Circuit
Figure 2

high speed, power peripheral drivers (2.0 A, 35-90 V) *designed for . . .*

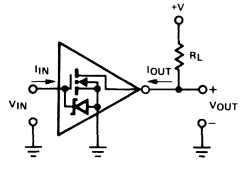
- **Peripheral Drivers for EDP and Process Control Systems**
- **Laser Diode Pulsing**
- **High Speed Line Drivers**
- **CMOS to High Current Interfacing**
- **TTL to High Current Interfacing**
- **Switching Reactive Loads**

BENEFITS

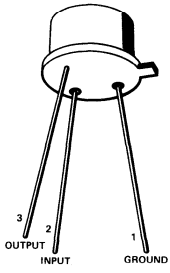
- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
  - Low Drive Current ($I_{GSS} < 100$ nA)
  - Threshold Voltage 0.8 to 2.0 V
- Fan Out From CMOS > 100
- No Power Supply Connection Required
- Permits Improved Data Transmission Times
  - Propagation Delay Typically 4 nsec
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - High Gain > 10 Meg @ 1.0 Amp
  - High Speed
  - Free From Failure Due to Secondary Breakdown and Thermal Runaway
  - Paralleled Easily Without Current Sharing Resistors
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

ABSOLUTE MAXIMUM RATINGS

Output Voltage	
S55V21	35 V
S55V02	60 V
S55V22	90 V
Continuous Output Current	2.0 A
Peak Output Current	3.0 A
Continuous Input Current	2.0 mA
Peak Input Current	100.0 mA
Voltage at Input	15 V
Reverse Input Voltage	−0.3 V
Power Dissipation at 25°C Case Temperature	6.25W
Storage Temperature	−55°C to 150°C
Operating Temperature	−55°C to 150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C



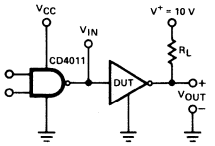
TO-39
See Section 4



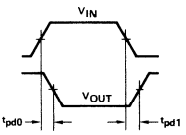
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

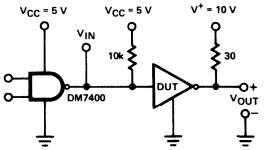
	Characteristic		S55V21			S55V02			S55V22			Unit	Test Conditions
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	V_{IN}	Logical "1" Input Voltage (Note 2)	4.0	2.0		4.0	2.0		4.0	2.0		V	I_O = 100 mA, V_{OUT} = 25 V
2			5.0	3.5		5.0	3.5		5.0	3.5			I_O = 300 mA, V_{OUT} = 25 V
3			10.0	6.5		10.0	6.5		10.0	6.5			I_O = 1 Amp, V_{OUT} = 25 V
4	V_{IN}	Logical "0" Input Voltage (Note 2)		1.2	0.8		1.2	0.8		1.2	0.8		I_O = 1.0 mA, V_{OUT} = 25 V
5				0.8			0.8			0.8			I_O = 0.1 mA, V_{OUT} = 25 V
6					0			0			0		I_O = 10 μA, V_{OUT} = 25 V
7	I_{IH}	Logical "1" Input Current		0.01	0.5		0.01	0.5		0.01	0.5	μA	V_{IN} = 10 V, V_{OUT} = 0
8	I_{IL}	Logical "0" Input Current (Note 2)		−0.01			−0.01			−0.01			V_{IN} = 0V, V_{OUT} = 25 V
9	V_{ON}	Output Breakdown Voltage	35			60			90			V	I_O = 10 μA, V_{IN} = 0
	Specifications For Use With CMOS (Figure 1)												
10	V_{OL}	Output ON Voltage (Note 1)		0.3			0.3			0.4		V	I_O = 100 mA, V_{IN} = 5 V
11				1.0	1.5		1.0	1.5		1.4	1.7		I_O = 300 mA, V_{IN} = 5 V
12				1.8	2.5		2.2	3.5		3.8	4.5		I_O = 1.0 Amp, V_{IN} = 10 V
13	t_{pd0}	Propagation Delay to Logical "0" Output (Note 2)		4	10		4	10		4	10	ns	Figure 1, R_L = 10 Ω, V_{CC} = 10 V
14				5			5			5			Figure 1, R_L = 30 Ω, V_{CC} = 5 V
15	t_{pd1}	Propagation Delay to Logical "1" Output (Note 2)		4	10		4	10		4	10		Figure 1, R_L = 10 Ω, V_{CC} = 10 V
16				5			5			5			Figure 1, R_L = 30 Ω, V_{CC} = 5 V
	Specifications For Use With TTL (Figure 2)												
17	V_{OL}	Output ON Voltage (Note 1)		0.3			0.3			0.4		V	I_O = 100 mA, V_{IN} = 5 V
18				1.0	1.5		1.0	1.5		1.4	1.7		I_O = 300 mA, V_{IN} = 5 V
19	t_{pd0}	Propagation Delay to Logical "0" Output (Note 2)		8			8			8		ns	Figure 2
20	t_{pd1}	Propagation Delay to Logical "1" Output (Note 2)		5			5			5			Figure 2

NOTES:
1. Pulse Test – 80 μs pulse, 1% duty cycle.
2. Sample Test.



CMOS Switching Circuit
Figure 1





TTL Switching Circuit
Figure 2

n-channel enhancement-mode VMOS Power FETs *designed for . . .*

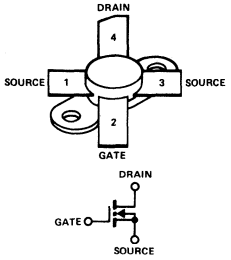
- **VHF Broadband Amplifiers**
- **Receiver Front Ends**
- **Class B, C, D, E Amplifiers**
- **Power Oscillators**

Performance Curves VMP4
See Section 3

BENEFITS

- Reduces Component Count and Design Time/Effort
  - Withstands Any VSWR
  - High Gain, 10 dB Min @ 200 MHz
  - High Two-Tone Intermodulation Intercept Point
  - Low Small Signal Noise Figure
  - Linear Transfer Characteristics
- Permits Broadband Designs
  - High Input Impedance
  - Low Noise Figure
- Permits Efficient Switching Amplifier Designs
  - High Input Impedance
  - No Storage Delay Time
  - Rise and Fall Time Typically 4 nsec
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases as Temperature Increases

380-SOE Flange
See Section 4



ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage . . . . . .60 V
Maximum Drain-Gate Voltage . . . . . .60 V
Maximum Gate-Source Voltage . . . . . .30 V
Maximum Continuous Drain Current . . . . . 2.0 A
Maximum Dissipation at 25°C Case Temperature . . . . . .25 W
Linear Derating Factor (Derate from 25°C) . . . . 200 mW/°C
Temperature (Operating and Storage) . . . . . .−55 to +150°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions	
1	S T	BV_{DSS}	Drain-Source Breakdown	60			V	V_{GS} = 0, I_D = 10 μA	
2		$I_{D(on)}$	ON-State Drain Current (Note 1)	400	600		mA	V_{DS} = 25 V, V_{GS} = 5V	
3	D Y N	g_{fs}	Forward Transconductance (Note 1)	170	240		m℧	V_{DS} = 24 V, I_D = 0.5 A	(Note 2)
4		C_{oss}	Common-Source Output Capacitance		34	37	pF	V_{GS} = 0, V_{DS} = 25, f = 1 MHz	
5		C_{iss}	Common-Source Input Capacitance		32	35			
6		C_{rss}	Reverse Transfer Capacitance		4.8	6.5			
7		G_{ps}	Common-Source Power Gain	10			dB	V_{DS} = 24 V, I_D = 0.2 A, f = 200 MHz	
8		NF	Small Signal Spot Noise Figure		2.5			V_{DS} = 24 V, I_D = 0.2 A, f = 150 MHz	

NOTES:
1. Pulse test – 80 μsec pulse, 1% duty cycle.
2. Sample test.

VNAR

n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Performance Curves VNAR
See Section 3

- **RF Power Amplifiers**
- **High Current Analog Switching**
- **Laser Diode Pulsing**
- **Bridge Switching**

ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage
- VN33AJ, VN35AJ . . . . . 35 V
- VN66AJ, VN67AJ . . . . . 60 V
- VN98AJ, VN99AJ . . . . . 90 V

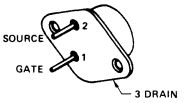
Maximum Drain-Gate Voltage
- VN33AJ, VN35AJ . . . . . 35 V
- VN66AJ, VN67AJ . . . . . 60 V
- VN98AJ, VN99AJ . . . . . 90 V

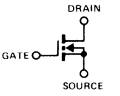
Maximum Continuous Drain Current . . . . . 2.0 A
Maximum Pulsed Drain Current . . . . . 3.0 A
Maximum Forward Gate-Source Voltage. . . . . 30 V
Maximum Reverse Gate-Source Voltage . . . . . 30 V
Maximum Dissipation at 25°C Case Temperature . . . . . 25 W
Linear Derating Factor . . . . . 200 mW/°C
Temperature (Operating and Storage) . . . . . −55 to +150°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

BENEFITS

- Reduces Component Count and Design Time/Effort
  - Withstands Any VSWR
  - High Gain, 10 dB Min @ 200 MHz
  - High Two-Tone Intermodulation Intercept Point
  - Low Small Signal Noise Figure
  - Linear Transfer Characteristic
- Permits Broadband Designs
  - High Input Impedance
  - Low Noise Figure
- Permits Efficient Switching Power Supply Designs
  - High Input Impedance
  - No Storage Delay Time
  - Rise and Fall Time Typically 4 nsec
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases As Temperature Increases

TO-3
See Section 4





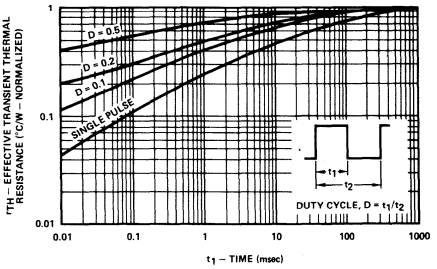
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		VN33AJ VN35AJ			VN66AJ VN67AJ			VN98AJ VN99AJ			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	BV_{DSS}	Drain-Source Breakdown	35			60			90			V	V_{GS} = 0, I_D = 10 μA
2		$V_{GS(th)}$	Gate-Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1 mA
3		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15 V, V_{DS} = 0
4						500			500			500		V_{GS} = 15 V, V_{DS} = 0, T_A = 125°C (Note 2)
5		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0
6						500			500			500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)
7					100			100			100		nA	V_{DS} = 25 V, V_{GS} = 0
8		$I_{D(on)}$	ON-State Drain Current	1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25 V, V_{GS} = 10 V
9		$V_{DS(on)}$	Drain-Source Saturation Voltage VN33AJ VN66AJ VN98AJ		1.0			1.0			1.1		V	V_{GS} = 5 V, I_D = 0.3 A
10						1.8			3.0			4.0		V_{GS} = 10 V, I_D = 1.0 A (Note 1)
11			VN35AJ VN67AJ VN99AJ		1.0			1.1			1.2			V_{GS} = 5 V, I_D = 0.3 A
12						2.5			3.5			4.5		V_{GS} = 10 V, I_D = 1.0 A
13		g_{fs}	Forward Transconductance	170	250		170	250		170	250		m℧	V_{DS} = 24 V, I_D = 0.5 A
14	DYNAMIC	C_{iss}	Input Capacitance		33	40		33	40		33	40	pF	V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz (Note 2)
15		C_{oss}	Common-Source Output Capacitance		38	45		35	40		32	40		
16		C_{rss}	Reverse Transfer Capacitance		7	10		6	10		5	10		
17		t_{on}	Turn ON Time		3	8		3	8		3	8	ns	See Switching Time Test Circuit VNAR, Section 3 (Note 2)
18		t_{off}	Turn OFF Time		3	8		3	8		3	8		

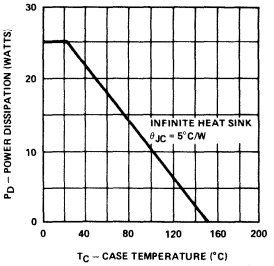
NOTES:
1. Pulse test—80 μs, 1% duty cycle.
2. Sample test.

VNAR

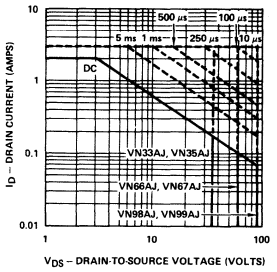
Thermal Response



Power Dissipation vs Case Temperature



Maximum Safe Operating Region



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

Performance Curves VNAR See Section 3

- **RF Power Amplifiers**
- **High Current Analog Switching**
- **Laser Diode Pulsing**
- **Bridge Switching**

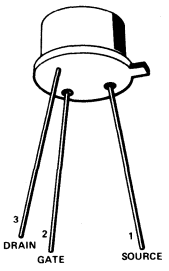
BENEFITS

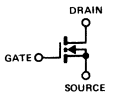
- Reduces Component Count and Design Time/Effort
  - Withstands Any VSWR
  - High Gain, 10 dB Min @ 200 MHz
  - High Two-Tone Intermodulation Intercept Point
  - Low Small Signal Noise Figure
  - Linear Transfer Characteristic
- Permits Broadband Designs
  - High Input Impedance
  - Low Noise Figure
- Permits Efficient Switching Power Supply Designs
  - High Input Impedance
  - No Storage Delay Time
  - Rise and Fall Time Typically 4 nsec
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Output Current Decreases As Temperature Increases

ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage	
VN33AK, VN35AK	35 V
VN66AK, VN67AK	60 V
VN98K, VN99AK	90 V
Maximum Drain-Gate Voltage	
VN33AK, VN35AK	35 V
VN66AK, VN67AK	60 V
VN98AK, VN99AK	90 V
Maximum Continuous Drain Current	2.0 A
Maximum Pulsed Drain Current	3.0 A
Maximum Forward Gate-Source Voltage	30 V
Maximum Reverse Gate-Source Voltage	30 V
Maximum Dissipation at 25°C Case Temperature	6.25 W
Linear Derating Factor	50 mW/°C
Temperature (Operating and Storage)	−55 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-39
See Section 4





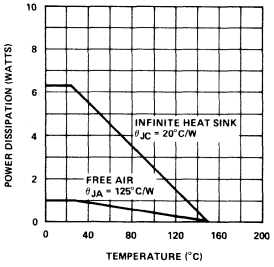
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		VN33AK VN35AK			VN66AK VN67AK			VN98AK VN99AK			Unit	Test Conditions	
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max			
1	STATIC	BV_{DSS}	Drain-Source Breakdown	35			60			90			V	V_{GS} = 0, I_D = 10 μA	
2		$V_{GS(th)}$	Gate-Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1 mA	
3		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15 V, V_{DS} = 0	
4						500			500			500		V_{GS} = 15 V, V_{DS} = 0, T_A = 125°C (Note 2)	
5		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
6						500			500			500		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
7					100			100			100		nA	V_{DS} = 25 V, V_{GS} = 0	
8		$I_{D(on)}$	ON-State Drain Current	1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25 V, V_{GS} = 10 V	
9		$V_{DS(on)}$	Drain-Source Saturation Voltage VN33AK VN66AK VN98AK		1.0			1.0					V	V_{GS} = 5 V, I_D = 0.3 A	(Note 1)
10						1.8			3.0			4.0		V_{GS} = 10 V, I_D = 1.0 A	
11			VN35AK VN67AK VN99AK		1.0			1.1			1.2			V_{GS} = 5 V, I_D = 0.3 A	
12						2.5			3.5			4.5		V_{GS} = 10 V, I_D = 1.0 A	
13		g_{fs}	Forward Transconductance	170	250		170	250		170	250		m℧	V_{DS} = 24 V, I_D = 0.5 A	
14	DYNAMIC	C_{iss}	Input Capacitance		33	40		33	40		33	40	pF	V_{GS} = 0, V_{DS} = 24 V, f = 1.0 MHz (Note 2)	
15		C_{oss}	Common Source Output Capacitance		38	45		35	40		32	40			
16		C_{rss}	Reverse Transfer Capacitance		7	10		6	10		5	10			
17		t_{on}	Turn ON Time		3	8		3	8		3	8	ns	See Switching Time Test Circuit VNAR, Section 3	(Note 2)
18		t_{off}	Turn OFF Time		3	8		3	8		3	8			

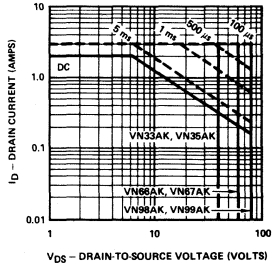
VNAR

NOTES
1. Pulse test—80 μs pulse, 1% duty cycle.
2. Sample test.

Power Dissipation vs Case or Ambient Temperature



Maximum Safe Operating Region



n-channel enhancement-mode VMOS Power FETs *designed for . . .*

- **High Speed Switching**
- **CMOS to High Current Interface**
- **TTL to High Current Interface**
- **High Frequency Linear Amplifiers**
- **Line Drivers**
- **Power Switching**

Performance Curves VNAZ See Section 3

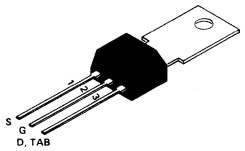
BENEFITS

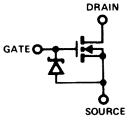
- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
- Permits More Efficient and Compact Switching Designs
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - Fan Out From CMOS Logic > 100
  - Easily Paralleled with Inherent Current Sharing Capability
  - High Gain
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Current Decreases as Temperature Increases
  - Input Protected From Static Discharge

ABSOLUTE MAXIMUM RATINGS

Maximum Drain-Source Voltage	
VN46AF	40 V
VN66AF	60 V
VN88AF	80 V
Maximum Drain-Gate Voltage	
VN46AF	40 V
VN66AF	60 V
VN88AF	80 V
Maximum Continuous Drain Current	2.0 A
Maximum Pulsed Drain Current	3.0 A
Maximum Continuous Forward Gate Current	2.0 mA
Maximum Pulsed Forward Gate Current	100 mA
Maximum Continuous Reverse Gate Current	100 mA
Maximum Forward Gate-Source (Zener) Voltage	15 V
Maximum Dissipation at 25°C Case Temperature	12.5 W
Linear Derating Factor	100 mW/°C
Temperature (Operating and Storage)	−40 to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

TO-202
See Section 4





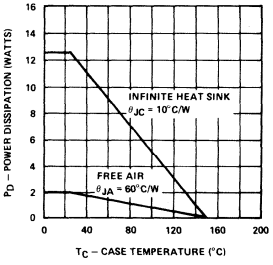
ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		VN46AF			VN66AF			VN88AF			Unit	Test Conditions
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
1	STATIC	BV_{DSS}	Drain-Source Breakdown	40			60			80			V	V_{GS} = 0, I_D = 10 μA
2				40			60			80				V_{GS} = 0, I_D = 2.5 mA
3		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1 mA
4		I_{GSS}	Gate Body Leakage		0.5	10		0.5	10		0.5	10	μA	V_{GS} = 10 V, V_{DS} = 0
5						500			500			500		V_{GS} = 10 V, V_{DS} = 0, T_A = 125°C (Note 2)
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10		V_{DS} = Max. Rating, V_{GS} = 0
7						500			500			500		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)
8					100			100			100		nA	V_{DS} = 25 V, V_{GS} = 0
9		$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25 V, V_{GS} = 10 V
10		$V_{DS(on)}$	Drain-Source Saturation Voltage (Note 1)		0.3			0.3			0.4		V	V_{GS} = 5 V, I_D = 0.1 A
11					1.0	1.5		1.0	1.5		1.4	1.7		V_{GS} = 5V, I_D = 0.3 A
12					1.0			1.0			1.3			V_{GS} = 10 V, I_D = 0.5 A
13					2.0	3.0		2.0	3.0		3.0	4.0		V_{GS} = 10 V, I_D = 1.0 A
14		g_m	Forward Transconductance (Note 1)	170	250		170	250		170	250		mℑ	V_{DS} = 24 V, I_D = 0.5 A
15	DYNAMIC	C_{iss}	Input Capacitance (Note 2)			50			50			50	pF	V_{GS} = 0, V_{DS} = 25 V, f = 1.0 MHz
16		C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10		
17		C_{oss}	Common-Source Output Capacitance (Note 2)			50			50			50		
18		$t_{d(on)}$	Turn-ON Delay Time (Note 2)		2	5		2	5		2	5	ns	See Switching Time Test Circuit VNAZ, Section 3
19		t_r	Rise Time (Note 2)		2	5		2	5		2	5		
20		$t_{d(off)}$	Turn-OFF Delay Time (Note 2)		2	5		2	5		2	5		
21		t_f	Fall Time (Note 2)		2	5		2	5		2	5		

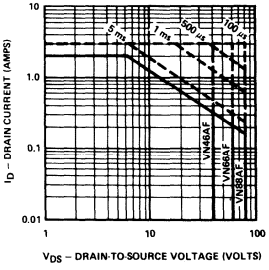
NOTES: 1. Pulse test – 80 μs pulse, 1% duty cycle.
2. Sample test.

VNAZ

Power Dissipation vs Case Temperature

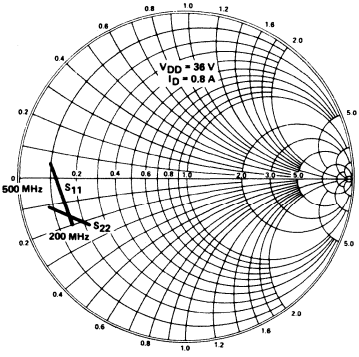


Maximum Safe Operating Region

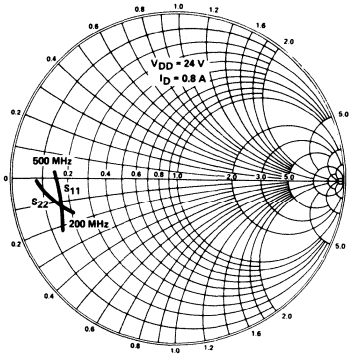


VMP4 PERFORMANCE CHARACTERISTICS

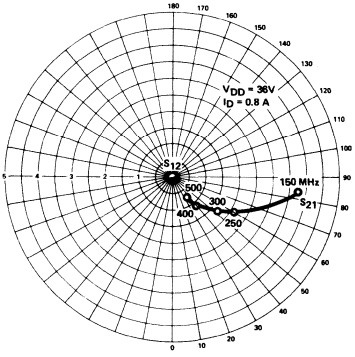
S_{11}/S_{22}



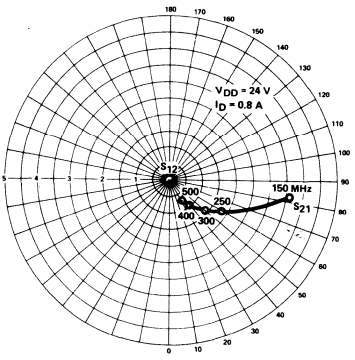
S_{11}/S_{22}



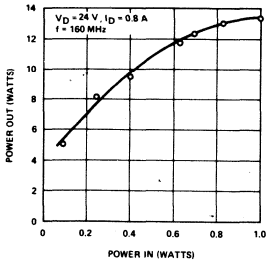
S_{21}/S_{12}



S_{21}/S_{12}

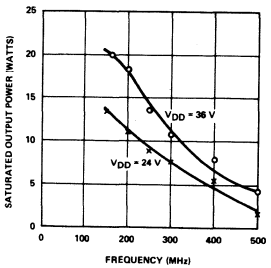


Output Power vs Input Power*



*Conjugate input/output match

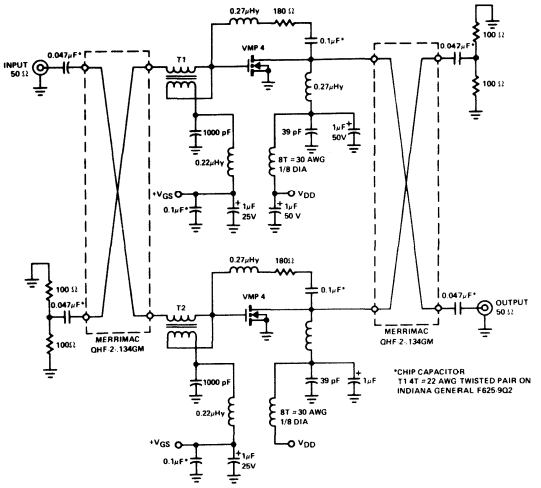
Saturated Output Power vs Frequency*
P_{IN} = 1 Watt, I_{DRAIN} = 0.8 A



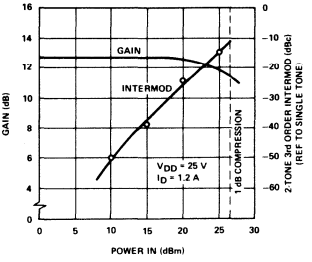
*Conjugate input/output match

VMP4 PERFORMANCE CHARACTERISTICS (CONT'D)

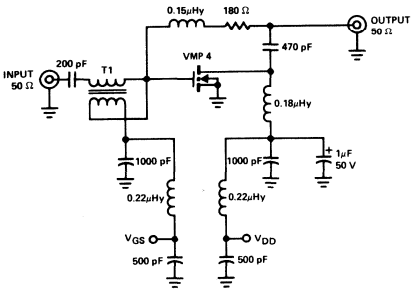
Quadrature Amplifier



Gain & 2-Tone 3rd Order Intermodulation Quadrature (100–160 MHz) Amplifier

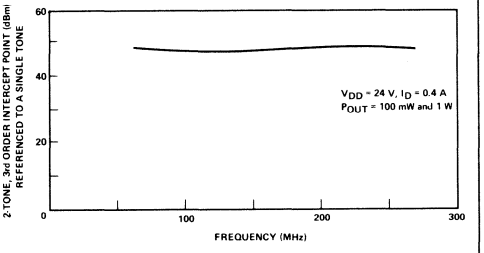


Broadband Amplifier

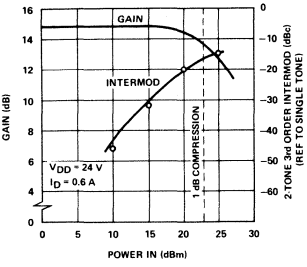


T1 4T #22 AWG TWISTED PAIR ON INDIANA GENERAL F625-9Q2

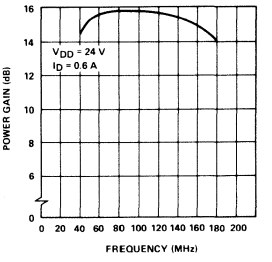
Broadband Amplifier Performance



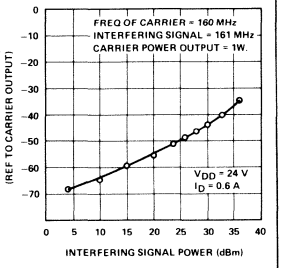
Gain and 2-Tone 3rd Order Intermodulation Broadband Amplifier



Broadband Amplifier



Effects of Interference

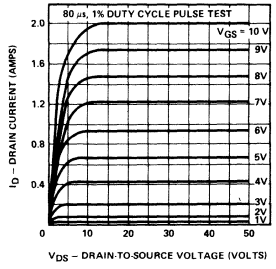


n-channel
enhancement-mode
VMOS Power FETs

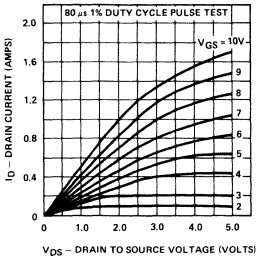
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-3	VN33AJ, VN35AJ, VN66AJ, VN67AJ, VN98AJ, VN99AJ
	TO-39	VN33AK, VN35AK, VN66AK, VN67AK, VN98AK, VN99AK
	380 SOE Flange	VMP4

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

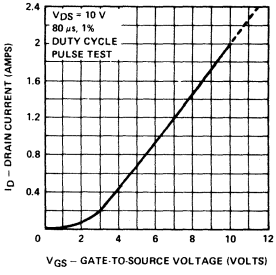
Output Characteristics



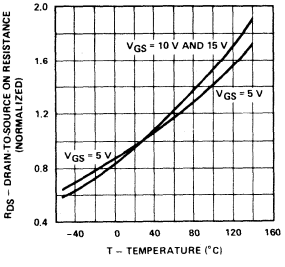
Saturation Characteristics



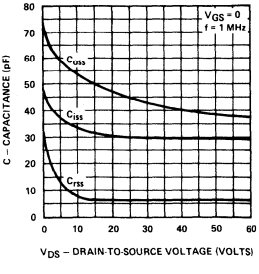
Transfer Characteristic



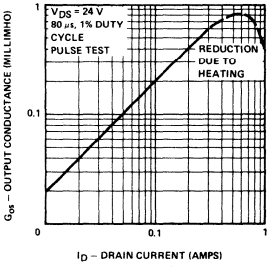
Normalized Drain-to-Source ON Resistance vs Temperature



Capacitance vs Drain-to Source Voltage

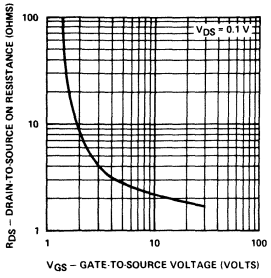


Output Conductance vs Drain Current

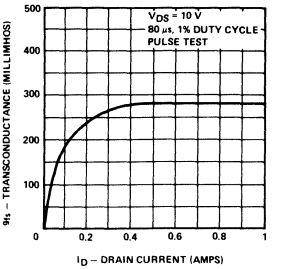


TYPICAL PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

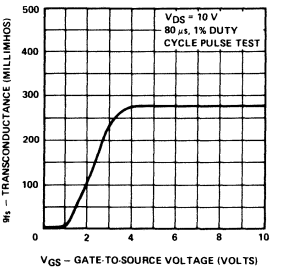
Drain-to-Source ON Resistance vs Gate-to-Source Voltage



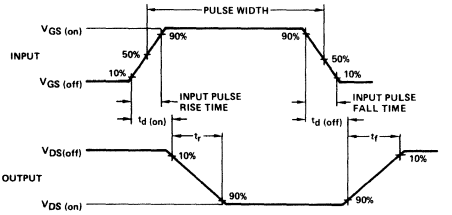
Transconductance vs Drain Current



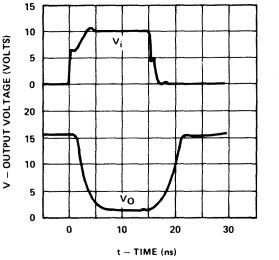
Transconductance vs Gate-to-Source Voltage



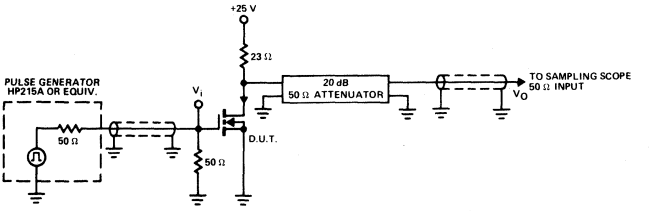
Switching Time Test Waveforms



Switching Waveforms



Switching Time Test Circuit

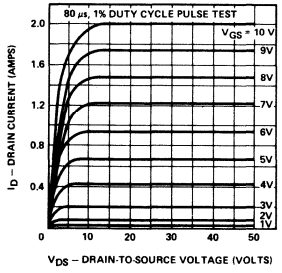


n-channel
enhancement-mode
VMOS Power FETs

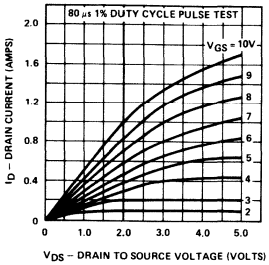
TYPE	PACKAGE	PRINCIPAL DEVICES
Single	TO-3	2N6656, 2N6657, 2N6658, S55V01, S55V11, S55V12
	TO-39	2N6659, 2N6660, 2N6661, S55V02, S55V21, S55V22
	TO-202	VN46AF, VN66AF, VN88AF

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

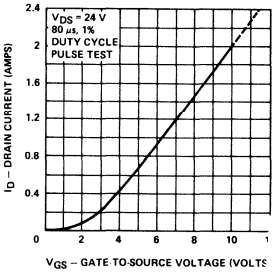
Output Characteristics



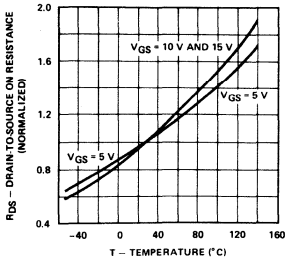
Saturation Characteristics



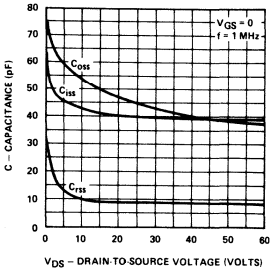
Transfer Characteristic



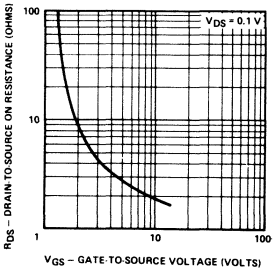
Normalized Drain-to-Source ON Resistance vs Temperature



Capacitance vs Drain-to-Source Voltage



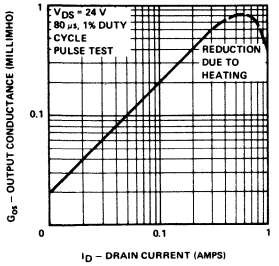
Drain-to-Source ON Resistance vs Gate-to-Source Voltage



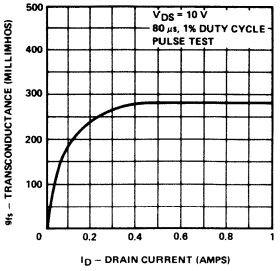
3

TYPICAL PERFORMANCE CURVES (Cont'd) (25°C unless otherwise noted)

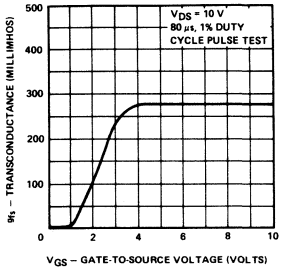
Output Conductance vs Drain Current



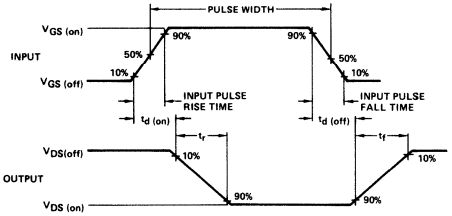
Transconductance vs Drain Current



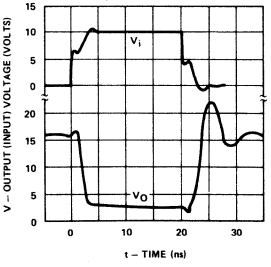
Transconductance vs Gate-to-Source Voltage



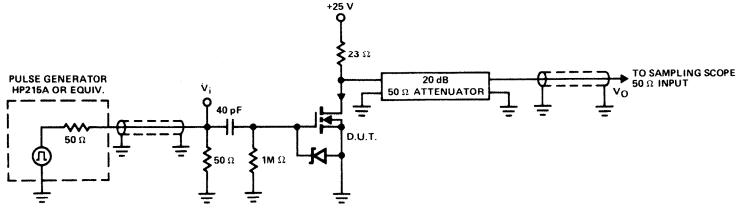
Switching Time Test Waveforms



Switching Waveforms

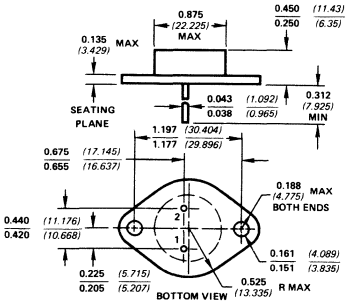


Switching Time Test Circuit

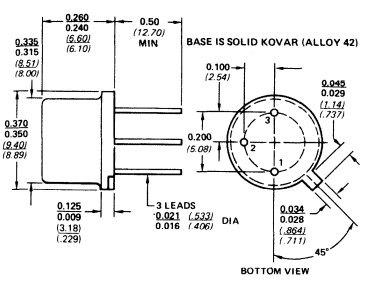


mechanical data

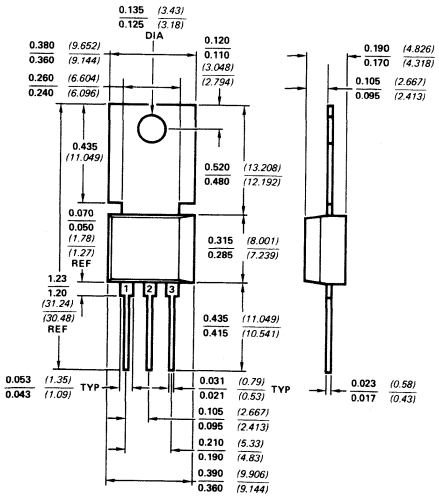
TO-3



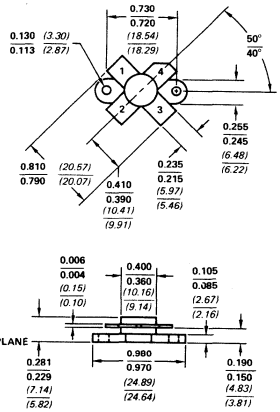
TO-39



TO-202



380-SOE Flange



ALL DIMENSIONS IN INCHES.
(ALL DIMENSIONS IN MILLIMETERS)

APPLICATION NOTE

VMOS-A Breakthrough in Power MOSFET Technology

Lee Shaeffer
Dave Hoffman
Revised

INTRODUCTION

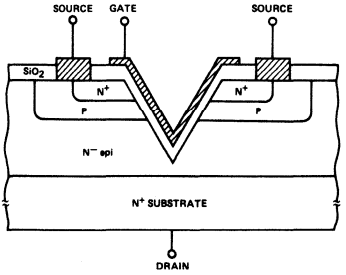
Until several years ago, Field Effect Transistors have been useful only at low (< 1 W) power levels. While possessing many theoretical advantages over their bipolar counterparts, the practical limitations in manufacturing high power devices precluded FET's competing with bipolar transistors and SCR's in power applications. A major limitation was that FET's were strictly horizontal devices, so their current densities were much less than the bipolar's (which utilized vertical current flow). For a given current, then, the FET chip area had to be considerably larger, which meant a lower yield and a resulting higher cost. Medium power FET's were therefore much costlier to fabricate than the bipolar counterparts, and high power FET's were even more impractical.

A new FET technology has recently been developed to increase current density and allow production of high voltage, high current FET's. This technology–VMOS, or Vertical MOS–exploits a diffused channel and vertical current flow to achieve its high power capabilities. Voltage and current levels compared to those of power bipolar devices are now feasible.

The VMOS Technology

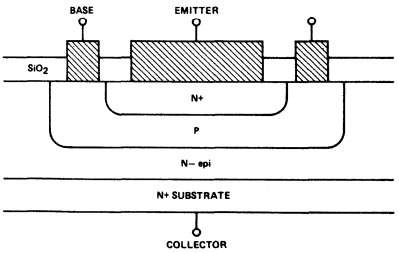
Figure 1 shows a cross section of a VMOS channel. The substrate, which eventually becomes the drain and provides a low resistance current path, is N^+ material. An N^- epi layer increases the drain-source breakdown voltage by absorbing the depletion region from the drain-body junction, which is normally reverse biased. Also, the epi layer greatly reduces the feedback capacitance since the gate overlaps N^- rather than N^+ material.

A P^- body and N^+ source are then diffused into the epi, followed by the preferential etching of a V groove through the source, body, and into the epi. Oxide is then grown and aluminum metalization deposited to form the source connection and gate. Finally, the entire chip is passivated to keep contamination (primarily sodium ions) from penetrating the gate oxide.



The Cross Section of a VMOS Channel
Figure 1

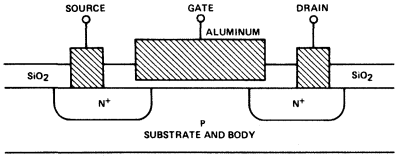
The processing, up to the point where the V groove is etched, is similar to that of the double-diffused epitaxial planar bipolar transistor, shown in Figure 2 for comparison.



A Double-Diffused Epitaxial Planar Transistor, Shown for Comparison
Figure 2

In operation, both the gate and drain are positive with respect to the source (and body). The gate produces an electric field which induces an N-type channel on both surfaces of the body facing the gate, allowing electrons to flow from the source, through the N-type channel, and epi, and into the substrate (drain). Because current flow—in the form of electrons—is entirely through N-type material, the VMOS is a majority carrier device. A greater gate voltage enhances a deeper channel, so the current path from the drain to the source is wider and current flow is increased. For example, the VN66AF VMOS FET conducts about 650 mA with 5 V between the gate and source, and 2 A with 10 V gate-to-source.

Figure 3 shows a conventional horizontal MOSFET. The N^+ source and drain are simultaneously diffused into the P-type substrate, which also serves as the body. Current flows horizontally from source to drain through the channel, which is induced on the top surface of the substrate.



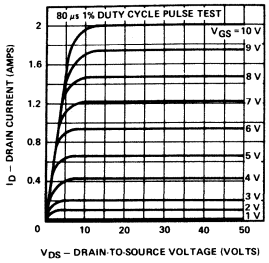
The Cross Section of a Conventional MOSFET
Figure 3

The vertical structure of VMOS gives it several important advantages over conventional MOS:

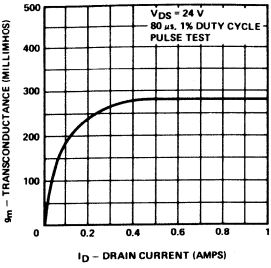
1. The length of the channel is determined by diffusion depths, which are much more controllable than the mask spacings used to define the channel length of conventional MOS, so the width/length ratio of the channel—which determines current density—is greater. For example, the length of the VN66AF channel is about 1.5 μm while in a conventional MOSFET it must be at least 5 μm to insure a good yield.
2. Each V groove creates two channels, so current density is inherently doubled, for each gate stripe.
3. The substrate forms the drain contact, so drain metal is not needed on top of the chip. This further reduces chip area and keeps the saturation resistance low.
4. The high current density of VMOS results in low chip capacitance, especially the feedback capacitance (gate-drain) since the overlap of the gate and drain are kept to a minimum. Extra gate-drain overlap must be allowed in conventional MOSFET's to guard against mask-misalignment, which increases the source-gate and gate-drain capacitance.
5. The VMOS epi layer absorbs the depletion region from the reverse-biased body-drain P-N diode, and therefore greatly increases the breakdown voltage while it has only a minimal effect on other device parameters (other than adding a series resistance). To fabricate a high voltage MOSFET the body region must be lightly doped so it can absorb the depletion region. The lightly doped material is very sensitive to oxide contamination and good long term stability is hard to achieve. Also, the gate oxide must be thick enough to withstand the entire gate-drain voltage (in VMOS it needs to stand off only about 1/4 of the gate-drain voltage) so a high voltage standard MOSFET lacks transconductance.

VMOS Characteristics

The output characteristics of the VN66AF, plotted in Figure 4, are similar to those of a conventional MOSFET with several exceptions. The vertical scale is amps rather than milliamps, the output conductance is low (the curves are flat rather than sloping) because of the buffering effect of the epi region, and the g_m is constant (the lines are evenly spaced) above 400 mA. The constant g_m, a characteristic of short-channel devices, is due to velocity saturation of the electrons in the channel—increasing the electric field intensity does not increase the drift velocity above a certain threshold. The g_m of a conventional (long channel) MOSFET, on the other hand, is proportional to the gate voltage; drain current is therefore proportional to the gate voltage; drain current is therefore proportional to $(V_{GS})^2$. Figure 5 is a more graphic illustration of the transconductance vs drain current for the VN66AF, showing the high linearity above 400 mA and the square law characteristics below 400 mA.



Output Characteristics of the VN66AF
Figure 4



Transconductance vs Drain Current of the VN66AF
Figure 5

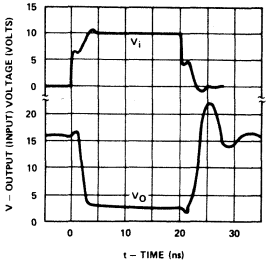
Of the advantages that VMOS has compared to bipolars, many are well known in small signal applications but many others are apparent only at higher power levels. They include:

1. High input impedance–low drive current (typically less than 100 nA). The "beta" of a VMOS device (the output current divided by the input current) is therefore over 10^9. Since the resultant drive power is negligible, VMOS will directly interface to medium high impedance drivers such as CMOS logic or opto isolators.
2. No minority carrier storage time. VMOS is a majority carrier device–its charge carriers are controlled by electric fields, rather than the physical injection and extraction (or recombination) of minority carriers in the active region. The switching delay time is small, several nanoseconds, and is caused primarily by external parasitic elements (series gate inductance). The 2N6657, for example, switches 1 A ON or OFF in 4 nsec, about 10 to 200 times faster than a bipolar.
3. No failure from secondary breakdown or current hogging. Since the temperature coefficient of the VMOS drain to source ON voltage is positive (a bipolar's is negative), VMOS draws less current as the device heats up. If the current density were to increase at one particular point of the channel, the temperature rises and the current decreases. The current automatically equalizes throughout the chip, so no hot spots or current crowding–which eventually leads to failure in a bipolar, can develop. Similarly, current is automatically shared between paralleled devices so no ballasting resistors are needed.

General Switching Applications

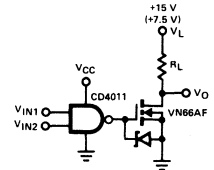
The high input impedance and high speed of VMOS makes it ideal as a switch–it will interface any driver capable of a 5V – 30V swing to nearly any load requiring several amps of current. Furthermore, the lack of failure from secondary breakdown means that it can withstand high voltage and high current simultaneously, so inductive loads are no problem.

The basic switching performance of the VN66AF is shown in Figure 6 while the corresponding test circuit is shown in Figure 7. The 2 nanosecond turn-ON and turn-OFF delay is caused by the input capacitance charging and discharging through the equivalent series inductance of the package and test jig.

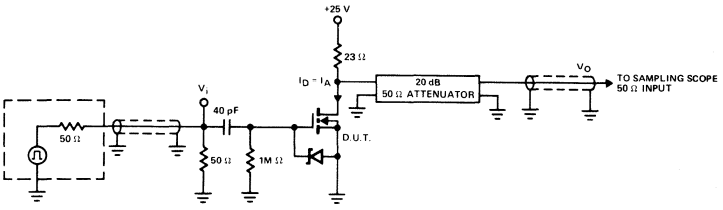


Switching Performance of the VN66AF
Figure 6

CMOS logic makes an ideal driver for the VN66AF, since no interface components are required (Figure 8). A logic low to the input of the CD4011 turns ON VN66AF (V_{GS} = 10 V), while a logic HIGH turns the device OFF (V_{GS} = 0). The steady-state power dissipated by the circuit, exclusive of load current, is a maximum of 55 μW (0.15 μW typ).



A CMOS Gate Driving the VN66AF
Figure 8



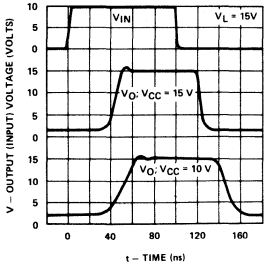
Switching Test Circuit for the VN66AF
Figure 7

Figures 9 and 10 depict the dynamic performance of the circuit shown in Figure 8 when the load is 13 Ω. V_L = 15 V when the logic supply voltage is 10 or 15 V (I_{LOAD} = 1A) and 7.5V for V_{CC} = 5 V (I_{LOAD} = 500 mA). The turn- ON and turn-OFF times when V_{CC} = 10 V are about 60 nsec; increasing V_{CC} to 15 V decreases switching times to 50 nsec, while decreasing V_{CC} to 5 V increases the switching times to 100 nsec. An examination of the output of the CD4011 reveals it is being loaded by 65 pF, the parallel combination of the input and Miller capacitances of the VN66AF.

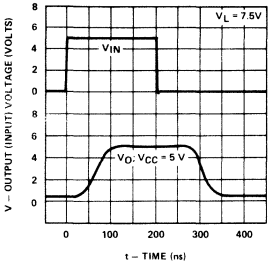
The switching speed is increased when several CMOS gates are paralleled to increase drive current to the VN66AF. For example, when four CD4011 gates are paralleled and V_{CC} is 15 V, switching times are about 25 nsec–most of it propagation delay through the CMOS gate (Figure 11).

Additional peak drive current to the VN66AF is needed to further decrease switching times, which is apparent when you consider that 50 mA of gate current is needed to charge or discharge the 65 pF effective input capacitance in 10 ns.

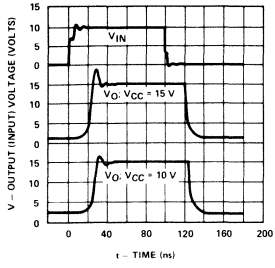
One solution is a MOS clock driver–it is designed to deliver high peak currents to capacitive loads and to translate TTL levels into 15 V swings. Figure 12 is a typical switching circuit whose characteristics are shown in Figure 13.

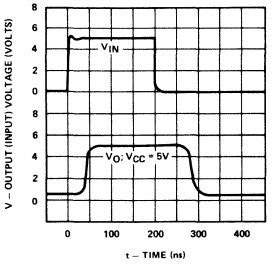


Switching Performance of the VN66AF Driven by the CMOS Gate in Figure 8
Figure 9

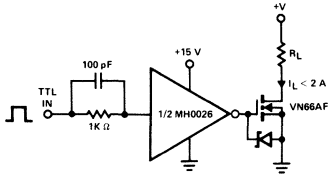


Switching Performance of the VN66AF With A 5 V CMOS Logic Drive
Figure 10

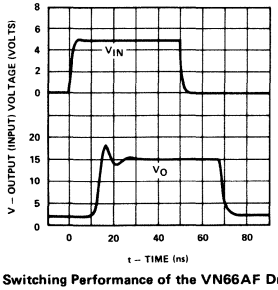




Switching Performance of the VN66AF Driven By Four Paralleled CD4011 Gates
Figure 11



Driving the VN66AF with a MOS Clock Driver
Figure 12

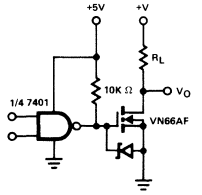


Switching Performance of the VN66AF Driven By a MH0026 MOS Driver
Figure 13

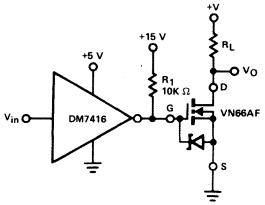
VMOS will also interface to standard TTL, but a pullup resistor is needed to insure sufficient gate enhancement (Figure 14). If no pullup resistor is used, the enhancement to the VMOS will be a mere 3V, and the VMOS will conduct only about 200 mA. On the other hand, with a full 5 V of enhancement on the gate of the VN66AF, it will conduct approximately 500 mA, which is sufficient for many applications.

If more current or a lower ON resistance is needed, more drive voltage must be applied to the VMOS. Figure 15 shows how to use open collector TTL with a 10 or 15 V supply, although now the turn-ON time will depend heavily on the value of R_1 since only it provides current to charge the input capacitance of the VN66AF. If an extremely fast turn-ON time is needed, R_1 must be very small and excessive power will be dissipated when the VN66AF is OFF. To solve this problem, use the totem pole drive circuit shown in Figure 16–it drives the VN66AF with an emitter follower, effectively reducing the capacitance that R_1 must charge (Figure 17).

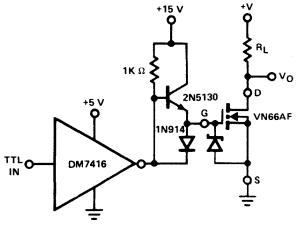
A second method of interfacing TTL to VMOS, the bipolar level shifter, shown in Figure 18, amplifies the TTL output pulse and provides up to 15 V of enhancement to the VN66AF. The AM686 is a high-speed comparator, although any comparator–or for that matter, any TTL gate–could be used instead. For a faster turn-ON time than that shown in Figure 19, or for a lower power dissipation in the OFF state, use the totem-pole driver.



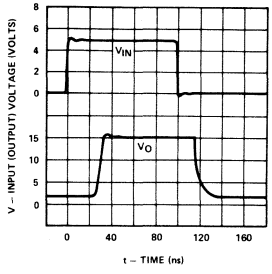
Driving the VN66AF With Standard TTL
Figure 14



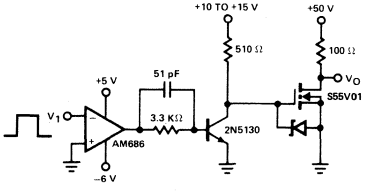
Open Collector TTL is Used to Provide Greater Enhancement to the VN66AF
Figure 15



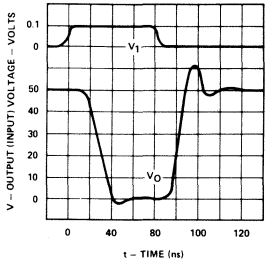
A "Totem Pole" Driver Increases Switching Speed and Reduces Dissipation
Figure 16



Switching Performance of the VN66AF Driven By the "Totem Pole" Open Collector TTL Driver
Figure 17



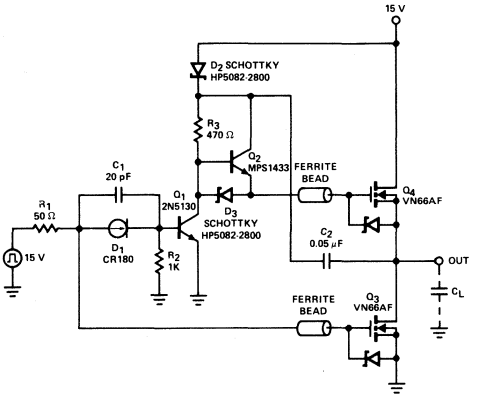
High Current Interface
Figure 18



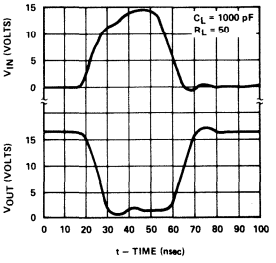
Performance of the High Current Interface
Figure 19

When driving capacitive loads, such as cables or data buses, an active pull-up is required to source current into the load. The high speed line driver shown in Figure 20 uses a second VN66AF with an inverter, to source up to 3 A and switch 15 V across 1000 pF in less than 15 ns. Bootstrap capacitor C_2 provides a 29 V drive to Q4–14 V greater than its source. Performance of the High Speed Line Driver is shown in Figure 21.

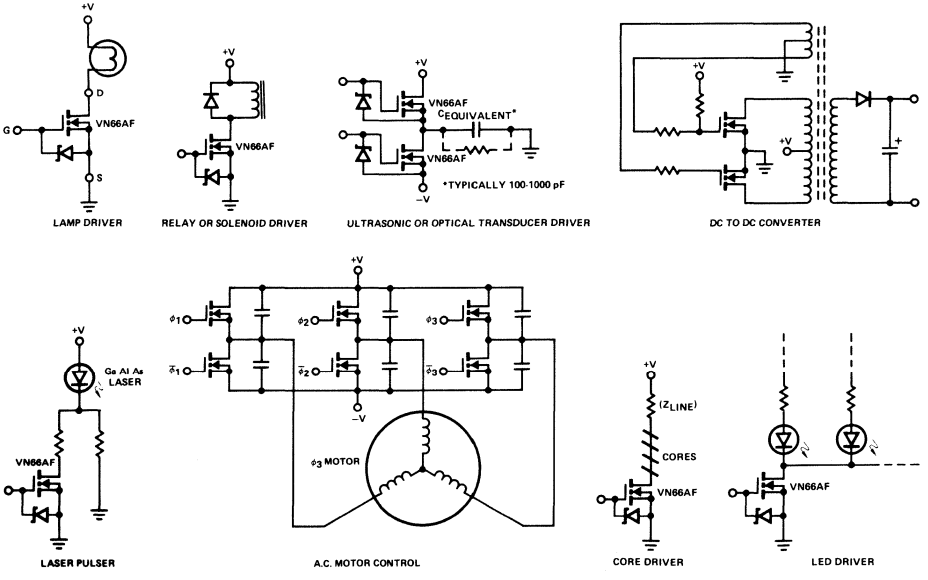
The ease of driving, ruggedness, lack of secondary breakdown and fast switch speeds make VMOS well suited for switching power to a variety of loads, some of which are shown in Figure 22.



High Speed Line Driver
Figure 20



Performance of the High Speed Line Driver
Figure 21



Several Typical VMOS Applications
Figure 22

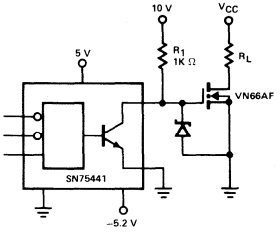
Interfacing VMOS to ECL is not quite as straightforward since ECL levels are inherently incompatible with VMOS drive requirements, but level shifting is still relatively easy. In Figure 23, the VN66AF is used to increase the voltage and current capability of the SN75441 30 V, 150 mA, ECL compatible peripheral driver. An alternate circuit, Figure 24, uses discrete components to translate ECL levels into the 0–10 V swing required for VMOS. Switching times of this circuit are less than 40 nsec into 50 Ω.[4]

The fast switching time of VMOS increases the efficiency of high-frequency switching regulators, since considerable power is lost while the switching element is traversing its active region. Figure 25 is the schematic of a 50 W, 200 KHz regulator using a 10 A, 60 V VMOS device.[5] The regulator output is 5 V at 5–10 A with a 28 V input; maximum output ripple is 100 mV p-p. No output current limiting is included, although it may be added depending on the need and the exact application.

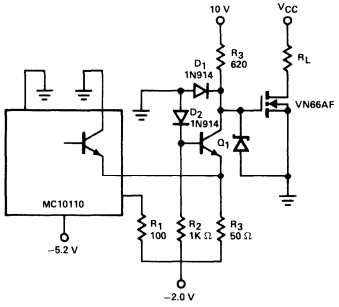
The LM710 comparator, which is offset 6 V from ground to eliminate the need for a negative supply, acts as a self-contained oscillator using L1 as a reactive element and R8 for hysteresis. C5 couples the output ripple to the negative input of the comparator, where it is rejected as a common mode signal. D4, R4, R5 and C1 form a bootstrap circuit which drives the gate 15 V more positive than the 28 V input rail. Six paralleled capacitors filter the output, since the total impedance of one capacitor at 200 KHz is 0.05 Ω and 0.01 Ω is needed to filter the 10 A peak-to-peak current. Q3 is the heart of a soft startup circuit.

Operation at 200 KHz, rather than the usual 20–25 KHz, has several advantages:

1. A smaller inductor, with lower DC (copper) losses, is needed.
2. A smaller filter capacitor is required.
3. The regulator responds faster to sudden changes in the load.

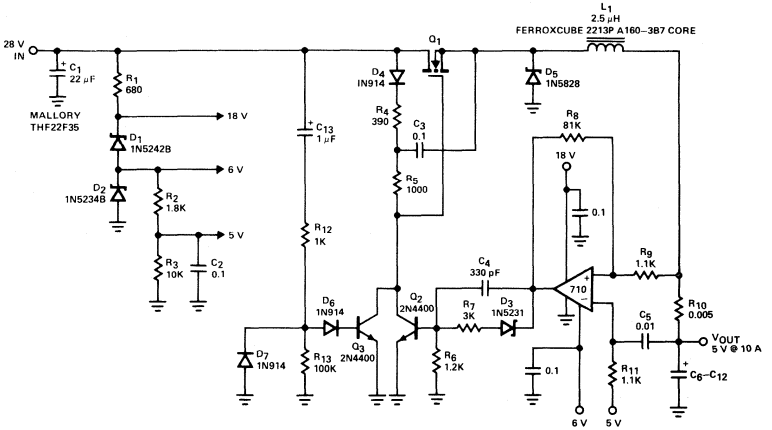


Using VMOS to Buffer the Output of an ECL Compatible Peripheral Driver
Figure 23



Q1 – USE A HIGH fT, RF BIPOLAR TRANSISTOR.

A Discrete ECL to VMOS Interface Circuit
Figure 24



A 200 KHz Switching Regulator
Figure 25

A Comparison of Four Regulators—28 V In, 5 V @ 10 A Out
Table 1

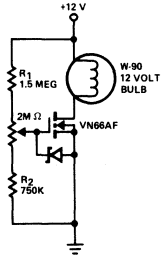
	20 kHz		200 kHz	
	BIPOLAR	VMOS	BIPOLAR	VMOS
Fixed Losses	4.85W			
Drive Power	0.17W	0.44W	1.4W	0.87W
Switching Losses	1.9	0.55	9.6	3.7
Saturation Losses	3.2	7.2	3.2	7.2
A.C. Core Losses	0.06		0.2	
D.C. Coil Losses	0.49		0.13	
Power Output	50.0	50.0	50.0	50.0
Total Input Power	60.7	63.6	69.4	67.0
EFFICIENCY	**82%**	**79%**	**72%**	**75%**

20KHz vs 200KHz for a 50 W Switching Regulator
Table 2

	20 kHz	200 kHz
Approximate Recovery Time for a 40% Change in Load	100 μsec	10 μsec
Inductor Core	3019 pot core ~0.85 in^3, 1.2 oz	2213 pot core ~0.31 in^3, 0.43 oz
Capacitors	8 x 220 μF 1.0 in^3	6 x 120 μF 0.45 in^3

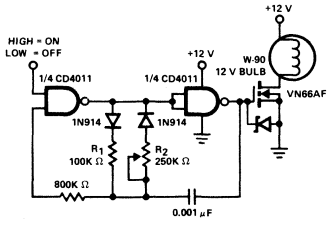
High frequency operation does reduce the overall efficiency somewhat, but not as much as it would in a comparable design using a bipolar or bipolar Darlington transistor as the switching element. Table 1 contains a comparison of both bipolar and VMOS regulators operating at 20 kHz and 200 kHz, while Table 2 compares the two different operating frequencies. A circuit topology similar to that of Figure 25 is assumed in all cases, although modifications to the basic circuit could further optimize the performances.

The high input impedance and linear transfer characteristic of VMOS makes it easy to control either the average or the surge current to the load. Figure 26 is a simple light dimmer circuit which varies the average current into the light bulb by controlling the saturation current of the VMOS. R_1 and R_2 make the control of brightness more linear with the potentiometer shaft rotation. The disadvantage of this circuit is that the VN66AF operates in its linear region, so considerable power is wasted when the light is dimmed.



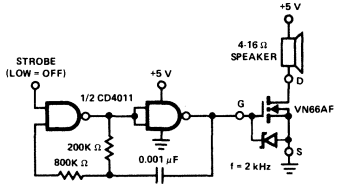
A Linear Light Dimmer Circuit
Figure 26

A more efficient method of varying the average current to the load is with pulse width modulation (Figure 27). The CD4011 oscillates with a duty cycle which is determined by the ratio of R_1 and R_2, and drives the VMOS with 12 V power. Since the VN66AF is either fully ON or fully OFF, very little power is dissipated in the regulator itself.



An Efficient Light Dimmer Circuit
Figure 27

A similar circuit can be used as an inexpensive audio alarm system. The CD4011 gates provide a 2 KHz square wave to the VN66AF, which directly drives an 8 Ω speaker (Figure 28).



A 2 KHz Audio Alarm
Figure 28

Drive Considerations

While the VN66AF can drive nearly any load of 2 A or less (3 A under pulsed conditions), the gate must be driven with a high enough enhancement voltage to support the required current. Refer back to Figure 4. If the VMOS is driven by TTL and the maximum V_{GS} is 5 V, a maximum drain current of 650 mA will flow regardless of the drain to source voltage. The typical worst case under these conditions is a drain current of 500 mA. If a minimum drain current of 1 A is required, a worst case minimum of 10 V must be applied to the gate (6.25 V will typically be sufficient).

Applying more than the minimum enhancement voltage, 15 V rather than 10 V, for example, has two desirable effects–the ON resistance is reduced, and an extra margin of safety is provided to allow for the decrease in drain current as the VN66AF heats up. It is possible, as the drain current decreases with temperature, for the VN66AF to actually come out of saturation and further increase its dissipation.

Temperature Considerations

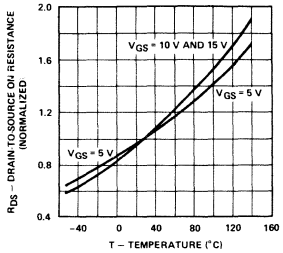
Typically, the $R_{DS(ON)}$ of VMOS increases 0.5 to 0.6%/°C due to the decrease in the mobility of electrons in silicon as temperature increases, which causes a proportional increase in drain-source voltage (Figure 29). If you assume a worst case situation of 0.6%/°C, the ON resistance at a given temperature ($R_{DS(T)}$) can be expressed in terms of the resistance at the ambient temperature ($R_{DS(T_A)}$) by the expression:[4]

$$R_{DS(T)} = R_{DS(T_A)} \bullet 0.006\ \Delta T \qquad (1)$$

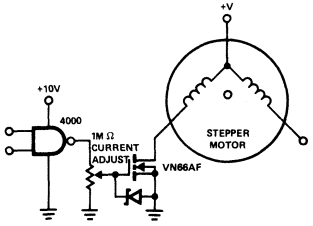
where $\Delta T = T - T_A$, the rise in temperature.

Many loads have undesirably high surge currents when power is first applied–motors and incandescent light bulbs, for instance. The soft-startup circuit in Figures 30 and 31 will minimize or eliminate these current surges,, which, in the case of the incandescent light bulb, will increase its life considerably. Adjust the 1M Ω potentiometer in Figure 30 until the desired maximum current is obtained, or use a fixed divider if a wider tolerance is allowable. R_1 and C_1 in Figure 31 have a 0.1 second time constant to increase the input drive voltage–and hence the drain current–of the VN66AF gradually.

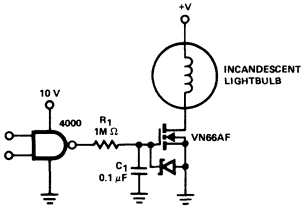
This increase in ON resistance may lead to problems unless certain design precautions are taken. In a typical switching situation, such as that of Figure 32, the current passing through the ON switch is nearly constant. In this example, one amp of current passes through the VN66AF and causes it to heat up. As the ON resistance goes up the voltage drop across the VN66AF increases, and the dissipation climbs further.



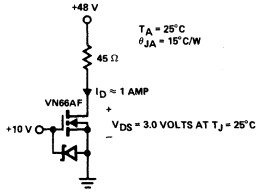
$R_{DS(ON)}$ vs Temperature of the 2N6660
Figure 29



A Circuit which Current Limits the Drive to the Motor
Figure 30



A Soft-Start-Up Circuit Reduces the Cold Current of the Bulb
Figure 31



A Typical Switching Circuit V_{DS} Increases as the VN66AF Heats Up
Figure 32

If inadequate heat sinking is used, the ON resistance and junction temperatures will increase until the resistance is stabilized by extra charge carriers which are thermally generated in the channel. Since this occurs above the maximum safe junction temperature of 150°C and the long term reliability may be impaired, it is desirable to anticipate this increase in ON resistance and temperature.

There are two ways to do this. The first, a rough rule of thumb, is to add an extra 50% to the actual power dissipation figure before calculating heat sink requirements. For example, if 1 A flows through a device whose ON resistance is 3 Ω at 25°C, the calculated power is 3 W. Now simply calculate the heat sink requirements using 4.5 W as the total dissipation to arrive at a close approximation of the actual heat sinking required at moderate and high temperatures (it will be conservative if the temperature rise is slight).

To calculate the heat sink requirements more precisely, express the rise in junction temperature, ΔT, in terms of the power dissipation and the junction to ambient thermal resistance, θ_{JA}:

$$\Delta T = I^2 R_{DS(T)} \theta_{JA} \qquad (2)$$

which can be combined with Equation 1 and rearranged as:

$$\Delta T\, e^{-0.006\Delta T} = I^2 R_{DS(T_A)} \theta_{JA}. \qquad (3)$$

This is the classical expression for the temperature rise of any fixed resistor, with the addition of the exponential term.

Solve Equation 3 with the values shown in Figure 29 to find the actual junction temperature.

$$\Delta T\, e^{-0.006\Delta T} = (1A)^2(3.0\ \Omega)(15°C/W)$$
$$= 45°C$$

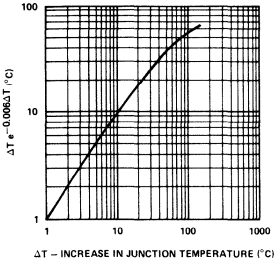
Next, find ΔT in Figure 33, by locating 45°C on the vertical axis. The actual rise in junction temperature, 70°C is located on the horizontal axis. T_J is therefore 95°C.

Figure 33, a plot of ΔTe–0.006ΔT vs ΔT, is useful in finding the actual temperature rise of the VN66AF when the power dissipation at 25°C junction temperature is known.

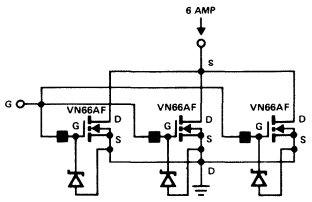
You can also use Figure 33 to find the required heat sinking when the power dissipation maximum allowable junction temperature is specified. For example, if the ambient temperature in Figure 29 is increased to 50°C, $R_{DS(T_A)}$ becomes 3.5 Ω and the normalized power 3.5 W. If the maximum junction temperature is specified as 125°C (ΔT = 75°C), ΔTe–0.006ΔT must be less than 48°C and $\theta_{JA} < 13.7°C/W$. A heat sink with $\theta_{JA} < -3.7°C/W$ should be used, since θ_{JC} of the VN66AF is 10°C/W. Note that if the rule of thumb were used and 50% added to the 3.5 W figure, the θ_{JA} would be calculated as 14.3°C/W, quite close considering the approximations involved.

Parallel and Series Operation

The current handling capability of VMOS may be increased quite easily by simply paralleling several devices (Figure 34). No ballasting resistors or thermal matching networks are needed because the currents tend to equalize. If a particular device starts to draw more current, it heats up more and conducts less current than it would otherwise. For example, an initial unbalance of ±20% (the typical worst case figure) will reduce to ±14% if the junction temperatures are allowed to approach their maximum limits. Because of the excellent high frequency response of the VN66AF, however, ferrite beads or small valued resistors (≈ 100 Ω to 1000 Ω) in series with each gate are necessary to suppress spurious high frequency (~300 MHz) oscillations.



A plot of $\Delta T\, e^{-0.006\Delta T}$ vs ΔT is useful in finding the actual temperature rise of the VN66AF when the power dissipation at 25°C junction temperature is known
Figure 33



Paralleling VN66AF's Increases the Maximum Current Handling Capability
Figure 34

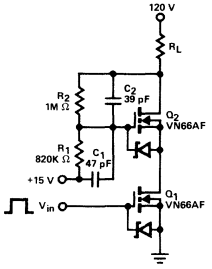
Devices may be connected in series to increase breakdown voltage, as shown in Figure 35. R_1 and R_2 are large because the drive current to the gate of Q_2 is small, while C_1 and C_2 form a capacitive divider which dynamically balances the gate drive and also insures fast switching times by converting charge to the gate of Q_2. C_1/C_2 should be approximately equal to R_2/R_1, with allowance for stray capacitance and the enhancement voltage of Q_2. The bottom of the divider chain is returned to 15 V, rather than ground, to insure sufficient enhancement for Q_2 when the devices are ON. By properly selecting resistor and capacitor values, any number of VMOS may be series connected in this manner.

Amplifier Applications

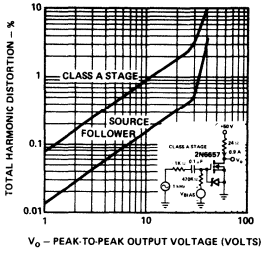
The constant g_m region of VMOS makes it well suited for linear applications, since distortion is low over a wide dynamic range when properly biased. Figure 36 is a graph of the harmonic distortion vs output voltage for a simple class A test circuit employing the 2N6657, a 25 W TO-3 version of the VN66AF. Inherent distortion rises almost linearly with output voltage at low signal levels, but then rises more sharply as the positive signal peaks extend into the non-linear g_m region and the negative peaks saturate the device. The gain of the circuit is about 6.5, equal to $g_m R_L$ (0.27 mmho x 24 Ω).

Using the 2N6657 as a source follower reduces the distortion by a factor of 5.5, which is slightly less than the amount by which the gain is reduced. Figure 37 shows that the frequency response of a simple class "A" stage is flat to almost 10 MHz.

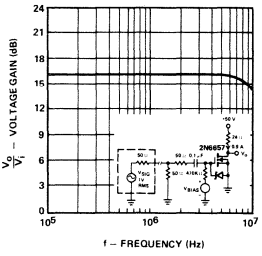
The simple audio amplifier shown in Figure 38 is equivalent to the audio output stage of many inexpensive radios, televisions, and phonographs. Power output is about 4 W from 100 Hz to 15 kHz. The design is greatly simplified by the use of an output transformer, and distortion is kept relatively low (2% at 3 W) by 10 dB of negative feedback. No thermal stabilization components are needed since the positive temperature coefficient of the drain-source ON voltage makes thermal runaway impossible.



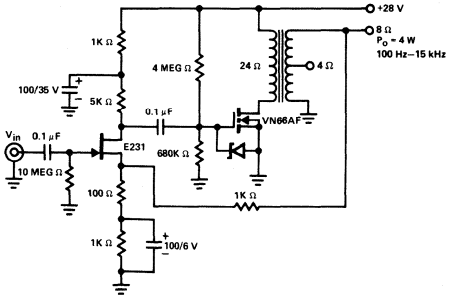
The Breakdown Voltage May Be Doubled By Connecting Device in Series
Figure 35



Harmonic Distortion vs Voltage Output for a Simple Class A Stage and a Source Follower
Figure 36



Frequency Response of a Simple Class A Stage
Figure 37

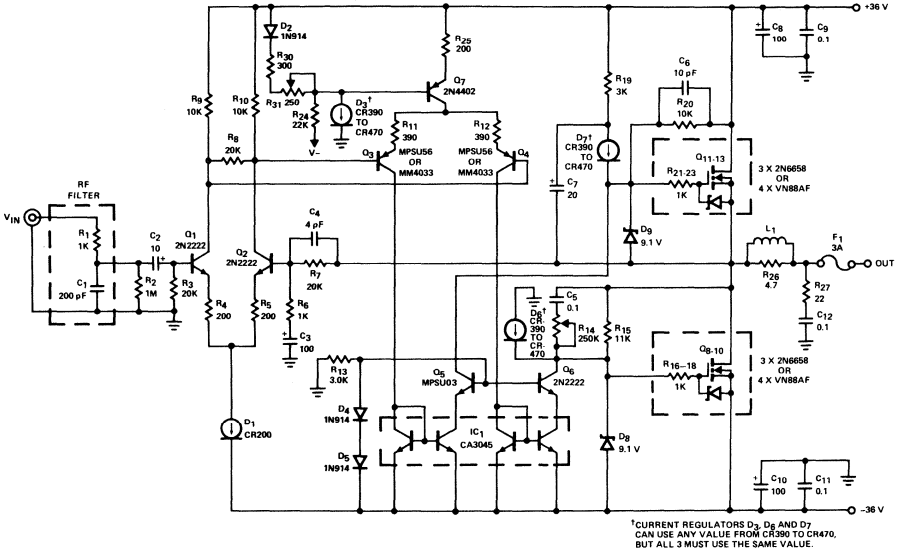


A Simple Audio Power Amplifier
Figure 38

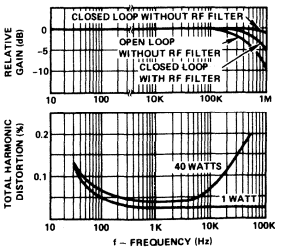
Figure 39 shows a high fidelity 40 W audio amplifier suitable for high quality stereo or quadraphonic systems. This amplifier has low open loop distortion, relatively small amounts of negative feedback (22 dB), and good open loop frequency response (400 KHz) to minimize transient intermodulation distortion. Closed loop frequency response (exclusive of the input filter) is flat to 4 MHz, and the slew rate is over 100 V/μs. The frequency response and performance of the amplifier, which is operated class AB with an idling current of 300 mA, are shown in Figure 40.

Since only N-channel VMOS devices are presently available, a quasi-complementary design is necessary and some means are required for matching the characteristics of the common source and common drain output stages.

The most effective method is to use a resistor (R_{15} in Figure 39) to provide local feedback from the drain back to the gate of the common source stage and then drive the gate with a modulated current source.



A High Quality 40 W VMOS Amplifier
Figure 39



Gain and Distortion vs Frequency of the VMOS Amp
Figure 40

Figure 41 depicts this technique and compares it to the corresponding circuit for an actual source follower. An analysis of the circuits reveals that both have the same values of gain and output impedance, which insures a good match between the positive and negative waveforms during class AB operation. Exact matching is insured by R_{14} and C_6 (Figure 39). Functional output protection is provided by the zener diode which limits the output current and device dissipation by limiting the gate enhancement. Clamping the gate-to-source voltage at a maximum of 9 V limits the drain current at slightly less than 2 A at 25°C, even less when the devices are hot. The resulting current limit versus the drain-to-source voltage, (Figure 42), shows that short circuit protection is possible when a 200°C max junction temperature is allowed for a brief interval (the time constant of the output fuse)

Complete construction plans for the amplifier, including a P.C. board layout, are available in the Siliconix Design Aid DA76-1, "The VMOS Power FET Audio Amplifier".

RF Power

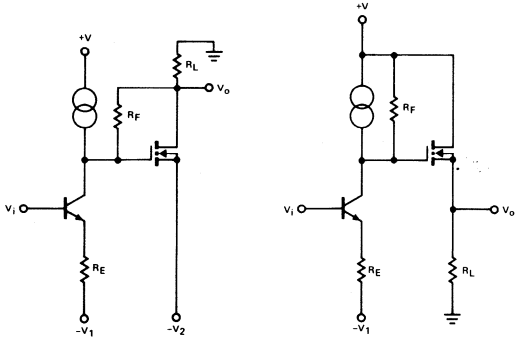
VMOS has many advantages in RF power amplifiers and pre-amplifiers, including high gain, a high two-tone intermodulation intercept point, low noise, and the ability to withstand any VSWR for further details, refer to TA76-1 and TA76-2.

SUMMARY

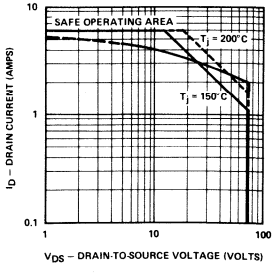
VMOS, a new Power MOSFET technology, relies on a short channel length and vertical current flow to increase current density and power capability. Its outstanding features include negligable DC drive current, extremely fast switching times, no minority carrier storage time, a complete lack of secondary breakdown and current hogging, and low distortion. VMOS devices are being designed into numerous power applications, including both general purpose and high speed switchers, high quality audio amplifiers and switching regulators.

REFERENCES

1. Hisashi Suwa and Alciyasu Ishitani, "Vertical Field Effect Transistor and It's Application to HIGH FIDELITY AMPLIFIERS", presented at the 51st convention of the Audio Engineering Society, May, 1975, AES Preprint No. 1018 (F-7).
2. Yoshida, Kubo and Ochi, "A High Power MOSFET with a Vertical Drain Electrode and a Meshed Gate Structure", IEEE Journal of Solid State Circuits, Volume SC-11, (August, 1976).
3. D. Hoffman, "VMOS Solves High Speed Line Driver Problems", (to be published).
4. L. Shaeffer, VMOS Peripheral Drivers, Solve Interface Problems", (to be published).
5. L. Shaeffer, "Improving Converter Performance and Operating Frequency with a New Power FET". Presented at the fourth National Solid-State Power Conversion Conference, May, 1977. From "Proceedings of Powercon 4/Boston, pp. C2-1 to C2-8.
6. L. Shaeffer, "Use FET's to Switch High Currents", Electronic Design 9, pp. 66-72 (April 1976).
7. L. Shaeffer, "Vertical MOSFET's (VMOS) in High Quality Audio Power Amplifiers", presented at the 54th convention of the Audio Engineering Society, May, 1976. AES Reprint No. 1106 F-8.
8. L. Shaeffer, 'The VMOS Power FET Audio Amplifier", Siliconix Design Aid DA76-1, May, 1976.



A Quasi Source Follower and a Real Source Follower
Figure 41



Current Output vs Drain-to-Source Voltage 3 2N6658's in Parallel, when V_{GS} = 9 V
Figure 42

APPLICATION NOTE

Don't Trade Off Analog Switch Specs. VMOS—A Solution to High Speed, High Current, Low Resistance Analog Switches

October 1977
Walt Heinzer

INTRODUCTION

For analog switches, Vertical MOS (VMOS) transistors give you a nearly ideal combination of characteristics—without the tradeoffs required by the more conventional components. These devices are now available from two American suppliers: Siliconix and its licensee, Semtech.

Unlike the commonly used N-channel JFETs, VMOS chips that handle more than a few hundred milliamps are also small enough for economical production. Smaller chips lead to lower inherent capacitances. Moreover, the basic VMOS structure provides lower ON resistance.

Some analog switches use relays, bipolar transistors and even triacs. Although electromechanical relays offer the lowest ON resistance initially, their ON resistance will vary with current and degrade with use. Also, relays suffer from mechanical limitations.

Bipolar transistors require base-drive current that causes offset in the switched analog signal. Triacs are only suitable for switching raw power; for analog switching, they introduce too much offset and non-linearity although they easily handle high power.

VMOS Offers High Performance

VMOS devices aren't limited by any of these disadvantages. They can switch 10 W, linearly, over a wide dynamic range. In addition, VMOS input impedance is very high, and only input voltage (no current) turns the transistors OFF or ON. And since the drain-to-source channel is purely resistive while ON, you get low distortion.

VMOS transistors in analog switches offer several more advantages, including

- 1.8 Ω ON resistance, which results in low insertion loss in low-impedance systems
- 2.0 A DC current capability—paralleling three VMOS devices increases this capability to 6.0 A and unlike other devices, paralleled VMOS do not require power-wasting ballast resistors
- 3 A peak current, which makes VMOS super for driving capacitive lines and quickly charging and discharging capacitors in high speed A/D converters, sample and hold circuits, and integrators
- 60 dB isolation at 10 MHz and 500 nA DC leakage in the OFF state
- Enhancement-mode operation with a 0.8 to 2.0 V threshold, which gives VMOS direct compatibility with CMOS and TTL. And the logic gates aren't loaded by the VMOS.
- Linear ON resistance, which results in low total harmonic and intermodulation distortion

What's more, all these capabilities come in a TO-202 package.

Examine the output characteristics of a low resistance VMOS device like the Siliconix VN46AF. A look at the transfer characteristic in Figure 1A reveals that varying the gate-to-source voltage from 0 to +10 V switches the VN46AF from OFF to ON–with a 3 Ω ON resistance. From the curve you can see that the device turns OFF well before zero volts, which eases interfacing with logic.

In the VN46AF schematic in Figure 1B, note that the body and source are internally connected. Figure 1C and 1D, respectively, show simplified models of the VN46AF's OFF and ON states. Diode D_1 is the body-to-drain PN junction. When the VN46AF is OFF, its drain current vs drain-to-source voltage characteristics (Figure 1E) is essentially the curve for D_1.

The breakdown for D_1 is 40 V, and the diode exhibits forward conduction for drain-to-source potential as low as –0.6 V. This diode therefore constrains the analog voltage, which a simple switch (one VMOS transistor) can handle, to between –0.6 and +40 V.

When the VN46AF is ON, a 2 Ω resistance is in parallel with D_1. Maximum continuous current in either direction is 2.0 A, even though the diode is forward-biased for currents over 0.5 A.

One VMOS Device Makes an Analog Gate

VMOS characteristics are put to good use in the analog switch of Figure 1F. In the ON state, the gate of the VN46AF is positive with respect to the source. In the OFF state, the gate-to-source voltage is zero. The 2.0 A capability and the 3 Ω ON resistance of the VMOS transistor can be fully exploited in this circuit. The input signal, however, is restricted to positive voltages and must always be greater than the output voltage. Otherwise, OFF isolation is impaired.

Both ON and OFF switching takes 200 ns; charge feed-through during the ON-to-OFF transition is 80 pC with a 50 Ω load. Charge transfer is, of course, especially important in sample and hold systems. For example, 80 pC into 0.01 μF causes an offset of 8 mV.

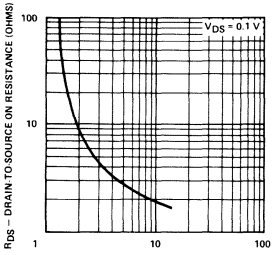
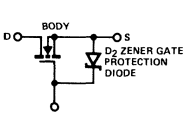
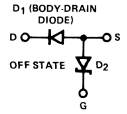


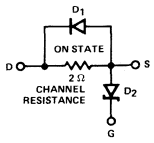
Figure 1A



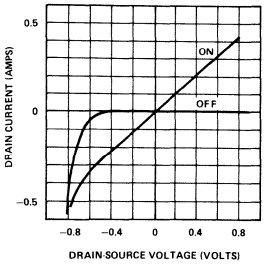
Schematic Symbol of VN46AF
Figure 1B



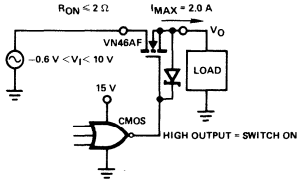
Equivalent OFF Condition (V_{GS} = 0)
Figure 1C



Equivalent ON Condition
(V_{GS} = 10 V)
Figure 1D



Small Signal Characteristics of VN46AF
Figure 1E



A Simple Unidirectional VMOS Analog Switch ($v_i \geq v_o$)
Figure 1F

The VN46AF switches from OFF to ON with a 3 Ω drain-to-source resistance, when its gate-to-source potential swings from 0 to +10 V. The device turns OFF at about 1 V(A). Some VMOS transistors (B) carry an on-board zener diode that protects the gate-to-source junction. A VMOS transistor is equivalent to two diodes in the OFF state (C), when the gate-to-source voltage is less than the threshold value. The equivalent diode, D_1 is shunted by 3 Ω when the VMOS device is ON (D), with the gate-to-source potential at +10 V. The small signal drain-to-source voltage vs current characteristic (E) is essentially determined by the body-to-drain diode. The input is restricted to positive voltages in the single-VMOS analog gate (F).

Figure 1

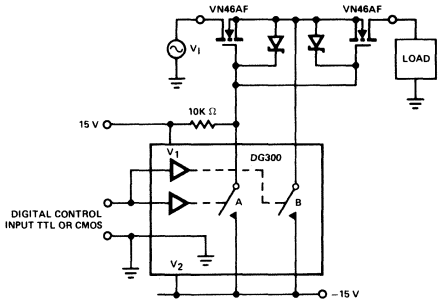
In Series, They Switch Both Polarities

To increase the switch's dynamic range, connect two VN46AF's in series (Figure 2A). In the ON state, both halves of the DG300 analog switch are open, so the gates of both VN46AF's are pulled to +15 V through the 10K Ω resistor. The ON resistance of this analog switch is twice as high as the drain-to-source resistance of a single VN46AF. The maximum current that this two-transistor switch can handle is the same as that for a single-transistor switch (2.0 A).

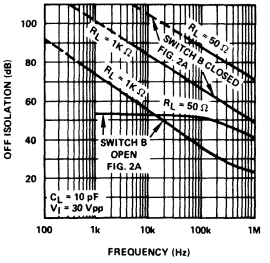
The switch is turned OFF by shorting the gates to the negative supply, thereby reducing the gate-to-source voltage to less than the threshold of 0.8 V. The second section of the DG300 adds 30 dB OFF isolation by shunting the signal-leakage path (through both sources) to the negative supply. OFF-isolation curves (Figure 2B) show that the DG300 raises the circuit's isolation and that decreasing the load resistance increases isolation.

Since the two transistors are back-to-back, one body-to-drain diode is always reverse-biased. This eliminates the OFF-state problem caused by forward-biasing the diode.

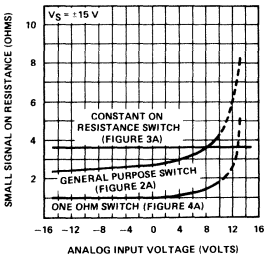
Since the bidirectional switch's gate drive is referenced to a fixed supply, its ON resistance varies with the input analog voltage (Figure 2C). This variation introduces distortion when you're driving low-impedance loads such as speakers or transmission lines. For constant ON resistance, use the circuit in Figure 3A.



A General Purpose Bidirectional Analog Switch
Figure 2A



OFF Isolation vs Frequency
Figure 2B



Small Signal ON Resistance vs Analog Input Voltage
Figure 2C

ON resistance is doubled in the two-VMOS switch (A), but inputs of both polarities are handled without losing isolation. The DG300 analog gate (B) raises the circuit's isolation by 30 dB. Decreasing load resistance also improves isolation. With the gate drive referenced to a fixed voltage (C), the ON resistance varies undesirably with the input, and generates distortion, especially with low impedance loads like speakers and transmission lines.

Figure 2

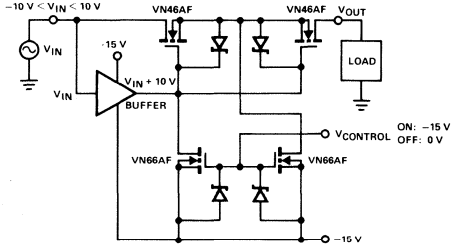
Bootstrapping Adds Linearity

In the ON state, a bootstrap voltage that tracks the input drives the gates of the VN46AF's. This bootstrapping keeps the VMOS's gate-to-source voltage constant and independent of the input signal. So, changes in the input-signal level do not modulate the ON resistance of the switch.

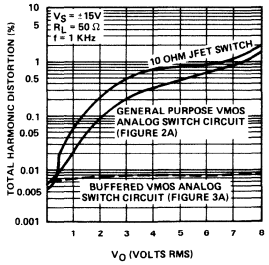
The buffer circuit reduces the computed total harmonic distortion from 1.5% to 0.005%, for 8 Vrms at 1 kHz into 50 Ω (Figure 3B). The popular 10 Ω DG186 JFET analog switch generates a higher total harmonic distortion of about 2%.

The two buffer circuits shown in Figures 3C and 3D isolate the input signal and employ a zener diode to provide a fixed gate-to-source voltage. The general-purpose buffer of Figure 3C has a flat frequency response of up to 300 kHz and accepts inputs ranging between ±15 V. The buffer of Figure 3D, VN66AK source follower, has its frequency response extended to 50 MHz and, when operated from ±30 V supplies, increases the signal range to ± 30 V.

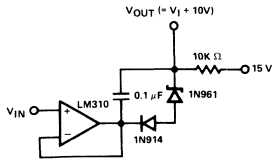
The VN66AK does not have an on-board zener diode like the VN66AF and VN46AF transistors. At the expense of the diode protection, the VN66AK gains lower capacitance from gate-to-source and reduced DC "see through" from driver to signal path. Bootstrapping the switch's gate circuits with a buffer permits the switch to operate with low distortion even as the signal amplitude comes close to the positive supply voltage.



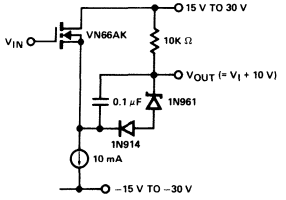
Low Distortion Constant ON Resistance Switch
Figure 3A



Distortion Improvement Using the Buffered Analog Switch
Figure 3B



General Purpose Buffer
Figure 3C



High Speed Buffer
Figure 3D

Bootstrapping the gate and input cuts distortion by holding the ON resistance constant (A). The buffered bootstrap circuit (A) distorts less than either a JFET or a nonbootstrapped VMOS analog switch (B). A general-purpose buffer (C) using the LM310 op amp is suitable for low speed switches, but when you need a fast analog switch, use the VN66AK buffer (D). In addition to speed, this buffer gives you increased isolation.

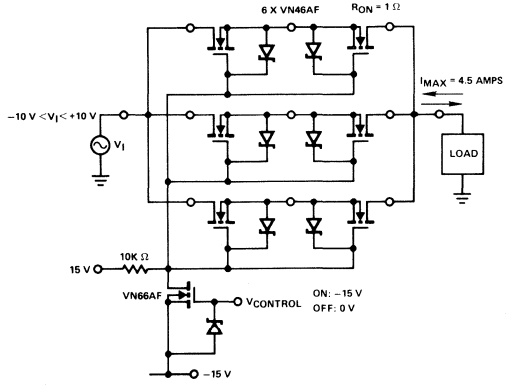
Figure 3

VMOS Devices Parallel Without Padding

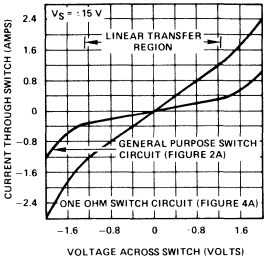
Paralleling devices lowers the total ON resistance. For example, three paralleled legs, each with two VN46AF's in series, make a 1 Ω switch (Figure 4A). Because VMOS devices are immune to current hogging, no ballast or balance resistors are needed. Negative tempcos, a VMOS feature, cause these devices to draw less current as they heat up. As a result, excess current is automatically shared by paralleled VMOS devices.

Paralleling three VN46AF's not only decreases ON resistance, but also increases the current capability to 6.0 A and extends the linear range of the large signal transfer characteristic from 0.3 to 1.2 A (Figure 4B).

The voltage range of the basic analog switch can also be increased. Simply use a higher breakdown VMOS unit (Figure 5). The VN98AK's have a 90 V breakdown, which allows up to ±40 V of voltage swing capability. However, these higher voltage devices do carry a penalty—the ON resistance is higher: 3.5 Ω vs 3.0 Ω for the VN46AF. Zener diode D_1 limits the gate-to-source potential to 30 V, and thereby prevents a possible gate-oxide rupture. Diode CR110 limits the current from the 50 V gate-bias supply.



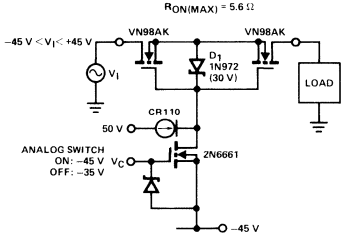
Ultra Low Resistance Switch (1 Ohm)
Figure 4A



Large Signal Transfer Characteristics
Figure 4B

No ballast or balance resistors are needed when VMOS devices are paralleled (A) because negative tempcos immunize them from current hogging. Paralleling extends the linear range from 0.3 to 1.2A (B) as it decreases the ON resistance of the analog switch to 1 Ω and increases its current-handling capability to 4.5 A.

Figure 4



90 V Peak to Peak Analog Switch

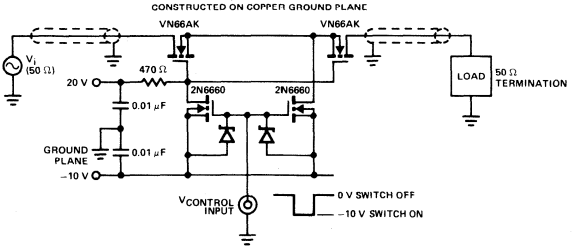
You pay for 90 V breakdown in the VN97AK with 3.0 Ω ON resistance, which allows swings of ±40 V. The zener diode limits the gate to-source potentials to 30 V.

Figure 5

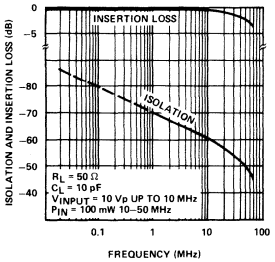
For the Ultimate in Switching Speed

The high power RF switch shown in Figure 6A performs very well up to 50 MHz–with turn-ON and turn-OFF times of 50 ns. At 10 MHz, isolation is 60 dB with a 20 V pk-pk input signal. Insertion loss is only 1 dB with a 50 Ω load (Figure 6B). The gain vs input power curve in Figure 6C shows that the RF analog switch using VN66AK's can put 1 W into a 50 Ω load at 14 MHz. The two-tone, third order, intermodulation product curves show a 42 dB intercept point with 1 dB of gain compression at 25 dBm input power.

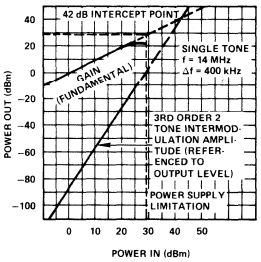
Turn-ON time of the switch (Figure 6D) is determined by the passive pull-up resistor combined with the capacitance at the gates of the VN66AK's. The negative turn-OFF transient is caused by charge-coupling to the output through the output capacitance of the VN66AK.



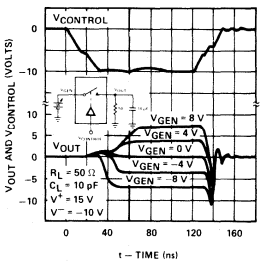
RF Analog Switch
Figure 6A



Insertion Loss and Isolation vs Frequency of RF Analog Switch
Figure 6B



Gain and Two Tone 3rd Order Intermodulation
Figure 6C



Switching Response of RF Switch into 50 Ohm Load
Figure 6D

The VN66AK switches high power at RF (A). At 10 MHz, a 20 V pk-pk signal is attenuated by 60 dB and the insertion loss is only 1 dB into 50 Ω and 10 pF (B). Third-order intermodulation distortion is given by the 42 dB intercept point, and 1 dB gain compression occurs at 25 dBm input for 14 MHz (C). The negative turn-OFF transient (D) is caused by charge-coupling to the output through the output capacitance of the VN66AK.

Figure 6

DESIGN AID

The VMOS Power FET Audio Amplifier

Lee Shaeffer
Revised September 1977

INTRODUCTION

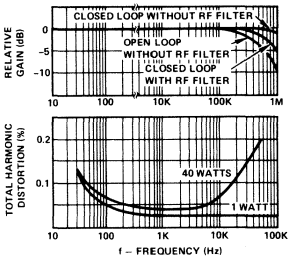
This Design Aid describes a high quality 80 watt stereo power amplifier using the 2N6658 VMOS FETs as output devices. This amplifier offers low harmonic distortion with relatively small amounts of negative feedback, and excellent transient response due to the good high frequency characteristics of the output FETs. Included in this Design Aid are a complete schematic, printed circuit board layout, component placement guide, construction suggestions, and parts list.

AMPLIFIER FEATURES

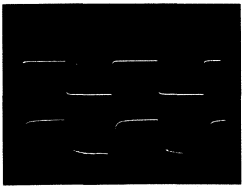
- 40 watts per channel into 8 Ω (clipping level 55 watts/channel)
- 1 Hz to 800 kHz response
- 0.04% typical distortion @ 1 kHz, 40 W
- >100 V/μs slew rate
- Output is short circuit protected

2N6658 FEATURES

- f_T = 600 mHz
- Linear g_m for I_D > 400 mA
- No Failure From Secondary Breakdown
- No Thermal Runaway
- Nearly Infinite Effective Beta



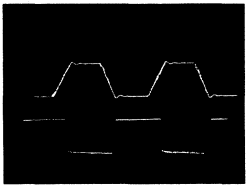
Gain and Distortion vs Frequency



10 kHz at 40 Watts into 8 Ω

100 kHz at 40 Watts into 8 Ω

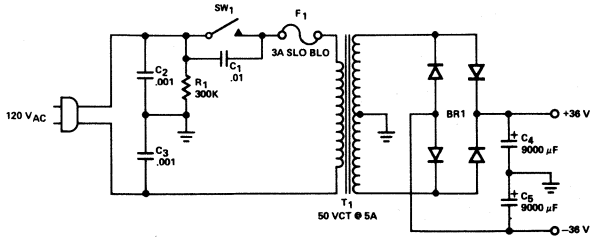
Amplifier Performance



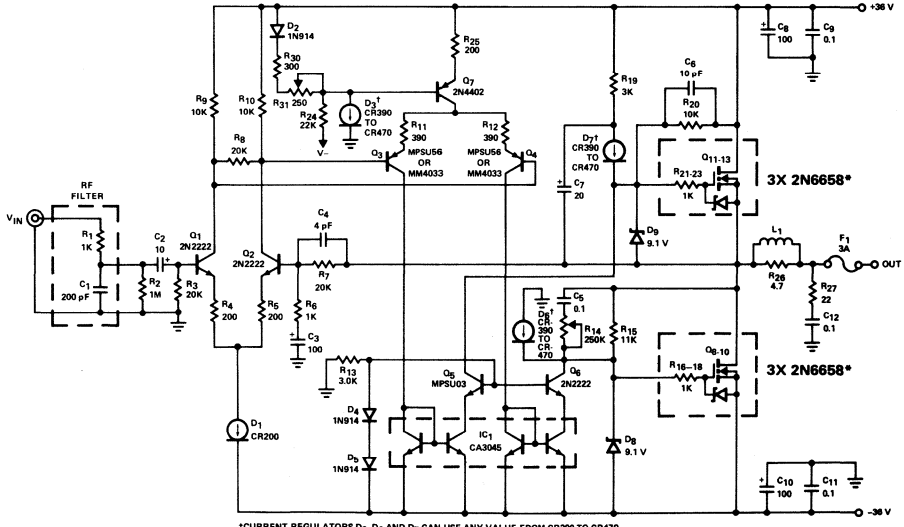
10 kHz at 32 V p-p into 2μF

100 kHz at 40 Watts into 8 Ω, Input Filter and Damping Network Disconnected

Amplifier Performance

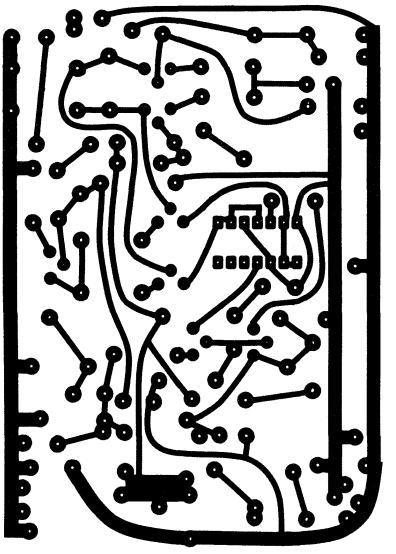


Schematic of The Power Supply

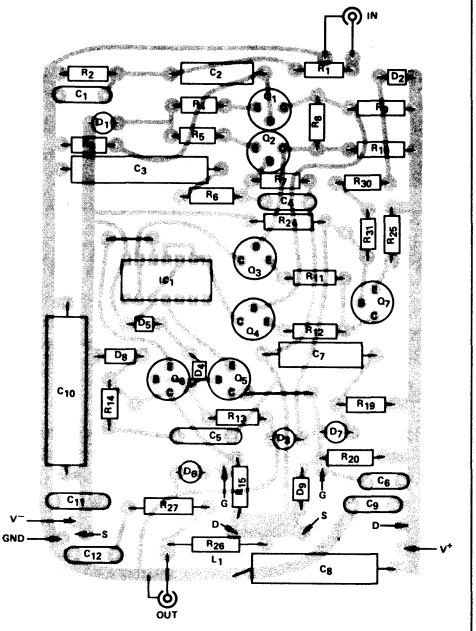


†CURRENT REGULATORS D_5, D_8 AND D_7 CAN USE ANY VALUE FROM CR390 TO CR470, BUT ALL 3 ON A PC BOARD MUST USE THE SAME VALUE.
*SIMILAR PERFORMANCE CAN BE OBTAINED USING PLASTIC POWER TAB TRANSISTORS. SUBSTITUTE 4 X VN88AF'S AND TO-202 HEAT SINKS FOR THE OUTPUT, KEEP THE SUPPLIES BELOW THE VN88AF 90V BV_{DSS}.

The Schematic of 1 Channel of the VMOS Power FET Amplifier



Printed Circuit Board
Bottom View
See page 5-24 for 1:1 copy

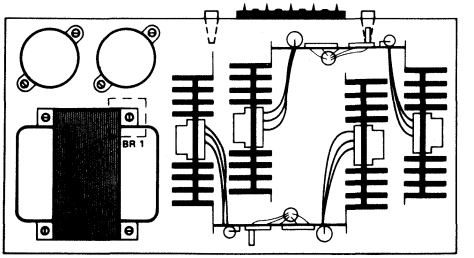


Layout (One Channel)
Top View – Components Layout

CONSTRUCTION SUGGESTIONS

IMPORTANT – R_{16} should be connected as close to the gate of Q_8 as practical (within 1 inch). Similarly, mount R_{17}, R_{18}, R_{21}, R_{22} and R_{23} close to the gates of Q_9–Q_{13}. Failure to do this may result in parasitic oscillations.

The entire amplifier may be mounted on a 7" x 13" x 2" chassis, as shown below. The heat sinks are mounted perpendicular to the P.C. board using spade lugs. The heat sinks from both channels are then interleaved, and mounted on the chassis with additional spade lugs. Input and output jacks should be mounted on insulated plastic or vectorboard and direct wired to the respective P.C. board.



Chassis Diagram

PARTS LIST – AMPLIFIER

The amplifier (one channel). All resistors are 1/4 W, 5% unless otherwise noted.

R_1	1K Ω
R_2	1M Ω
R_3	20K Ω
R_4, R_5	200 Ω
R_6	1K Ω
R_7, R_8	20K Ω
R_9, R_{10}	10K Ω
R_{11}, R_{12}	390 Ω
R_{13}	3.0K Ω, 1/2 W
R_{14}	250K Ω Trimmer
R_{15}	11K Ω
R_{16}-R_{18}	1K Ω (Not shown on P.C. board layout diagram, mounted on heat sinks.)
R_{19}	3K Ω
R_{20}	10K Ω
R_{21}-R_{23}	1K Ω (Not shown on P.C. board layout diagram, mounted on heat sinks.)
R_{24}	22K Ω
R_{25}	200 Ω
R_{26}	4.7 Ω, 2 W
R_{27}	22 Ω, 2 W
R_{30}	300 Ω
R_{31}	250 Ω Trimmer
C_1	200 pF
C_2	10 μF, 6 V
C_3	100 μF, 6 V
C_4	4 pF, 300 V
C_5	0.1 μF, 100 V
C_6	10 pF, 300 V
C_7	20 μF, 100 V
C_8	100 μF, 50 V
C_9	0.1 μF, 100 V Ceramic
C_{10}	100 μF, 50 V
C_{11}, C_{12}	0.1 μF, 100 V Ceramic
L_1	1 layer of #26 wire wound around R_{26}
F_1	3 Amp fuse (Not shown on P.C. board layout diagram)
D_1	CR200 2 mA Current Regulator Diode (Siliconix)
D_2	IN914 Silicon Diode
D_3†	Current Regulator Diode (Siliconix) CR390 to CR470 (3.9 to 4.7 mA)
D_4, D_5	IN914 Silicon Diode
D_6, D_7†	Current Regulator Diode (Siliconix) CR390 tp CR470 (3.9 to 4.7 mA)
D_8, D_9	9.1 V 500 mW Zener (Motorola IN5855B)
Q_1, Q_2	2N2222
Q_3, Q_4	MPSU56 or MM4033 (Motorola)
Q_5	MPSU03 (Motorola)
Q_6	2N2222
Q_7	2N4402
Q_8–Q_{13}*	2N6658 (Siliconix) (Not shown on P.C. board layout diagram, mounted on heat sinks.)
IC_1	CA3045 (RCA)
Heat Sink*	1 Wakefield 410K + 1 Wakefield 403K stacked or 1 Thermalloy 6401B + 1 Thermalloy 6430B stacked on top of each other to accomodate 3 TO-3 packages.
Misc.	Mounting Hardware

PARTS LIST – POWER SUPPLY

R_1	300K 1/2W, 5%
C_1	0.01 μF 600 V Ceramic
C_2, C_3	0.001 μF 600 V Ceramic
C_4, C_5	9000 μF 50 V Electrolytics (Cornell-Dubilier FAH9000-50-B3)
BR_1	12 A 100 V Rectifier Bridge (Motorola MDA980-2)
T_1	50 VCT at 5A (Triad F-58A)
F_1	3 Amp Slo Blo Fuse
SW_1	SPST 10A 250 V Toggle Switch
Misc.	Line cord, chassis, and assorted screws, nuts, and washers.

† Current regulators D_3, D_6 and D_7 can use any value from CR390 to CR470, but all 3 on a PC board must use the same value.

* Similar performance can be obtained using plastic power tab transistors. Substitute 4X VN88AF's and TO-202 heat sinks for the output, keep the supplies below the VN88AF 80 V BV_{DSS}.

INITIAL ADJUSTMENTS

1. A current limited (500 mA–1 Amp) power supply should be used for the initial power up sequence. If none is available, connect 100 Ω, 10 watt resistors in series with the VMOS drains.

2. R_{14} and R_{31} should be set to their maximum values (fully counter clockwise).

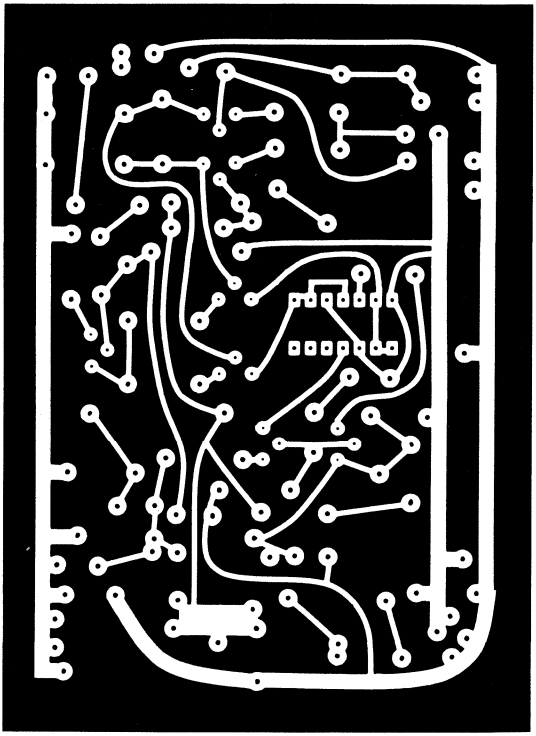
3. Monitor the current in series with the positive supply, and the voltage at the output. When power is initially applied, the supply current should be about 40 mA, and the output voltage nearly zero.

4. Slowly turn R_{31} clockwise until the supply current starts to increase. Allow the amplifier to warm up for 5 minutes, then set R_{31} for an idling current of 200–350 mA (the minimum distortion is at about 300 mA).

5. The regular power supply can now be connected. The idling current should remain the same. If not, readjust R_{31}. (If a large charge in R_{31} is needed, the amplifier may not be working properly.)

6. If a distortion analyzer is available, set the output power at 10 watts, 1 kHz. Adjust R_{14} for minimum distortion. A definite dip should be noticed. If no distortion analyzer is available, set R_{14} at midrange (≈125K).

7. When the above procedures have been followed for both channels, connect the VMOS Power FET amplifier to your favorite speakers and enjoy!



Scale, 1:1

Circuit Board
(Bottom View)

TECHNICAL ARTICLE

VMOS Power FETs in your next Broadband Driver

Ed Oxner

INTRODUCTION

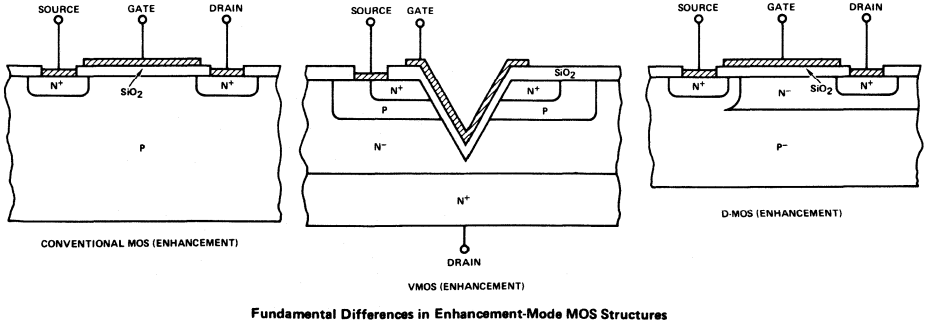
The VMOS Power FET introduced by Siliconix incorporated in 1976, is undoubtedly the most revolutionary semiconductor in decades and one that will open up exciting new applications heretofore impossible with bipolar transistors. Switching 1 ampere currents in less than 4 nanoseconds is commonly accomplished with this new power MOSFET. Among the many new features is one in particular that will interest those who seek for wide dynamic range: A linear transfer characteristic! Imagine, too, a transistor that can double for either a linear power amplifier or a wide dynamic range, low-noise, small-signal, front-end transistor!

Other features of the VMOS Power FET are typical for field-effect transistors and especially desirable for power transistors. Like all FETs, there is no thermal runaway nor secondary breakdown, and no minority carrier storage time. The latter opens up interesting applications for class D (switching) amplifiers. Additionally, the VMOS Power FET can accept any VSWR – open or short at any phase without any debilitating effects. Being an enhancement mode, N-Channel MOSFET one can operate in any class (A, AB, B or C) without needing negative power supplies for bias; zero bias providing class C service.

What is a 'VMOS Power FET'?

Unlike the usual MOSFET which is 'planar' in construction, the VMOS Power FET is a 4-layered vertical structure shown in comparison in Figure 1. This figure compares, somewhat oversimplified, the fundamental differences between MOS, DMOS and VMOS – which is the generic name for the VMOS Power FET structure. Common to both MOS and DMOS (*not* VMOS) is the singular disadvantage which affects their power handling capabilities: The geometry requires massive area to handle the current necessary for power. A further disadvantage lies in their inability to accept high voltages. In the VMOS Power FET, the current travels vertically, the source being on the top while the drain is the backside of the chip. In this vertical structure are 4 layers (N+/P/N–/N+) whose dimensions are precisely controlled by diffusion processes rather than by the less precision photolithographic methods common to the planar (MOS) technology.

VMOS offers high current densities, high source-to-drain breakdown capability and low gate-to-drain feedback capacity which makes the VMOS Power FET a great power transistor for HF and VHF applications. Probably the most



Fundamental Differences in Enhancement-Mode MOS Structures
Figure 1

attractive aspect of this revolutionary semiconductor is its inherent linear transfer characteristic. In conventional MOSFET (and JFET) this transfer characteristic is closely identifiable to a square-law response; that is, the drain current is proportional to the square of the gate-to-source voltage. However, in the VMOS structure the short channel causes the drain current to be linearly proportional to the gate-to-source voltage. Figure 2 provides a plot showing this effect.

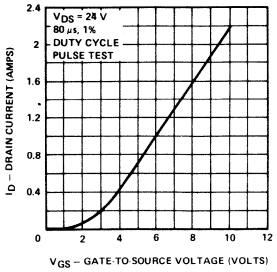
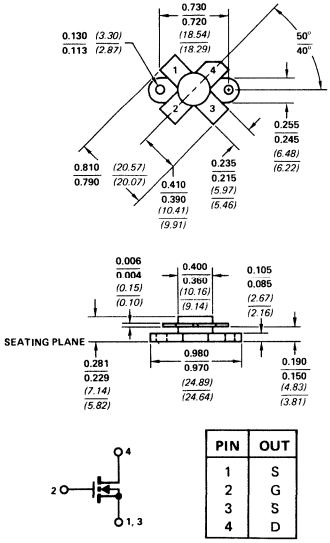


Figure 2

The VMOS Power VHF FET: VMP 4

Packaged in the popular flange mount, 'opposing emitter' (in this case, opposing source) strip-line configuration (Figure 3) is the Siliconix VMP 4 capable of saturated output power approaching 20 watts at 160 MHz. The performance shown in Figure 4 represents the available *saturated* output power versus frequency when both the input and output impedances of the VMP 4 are conjugately matched, *not* in the circuit described in this article. Unlike the more widely used JFET (or MOSFET) the input and output impedances (in common source configuration) are particularly suited for



PIN	OUT
1	S
2	G
3	S
4	D

Figure 3

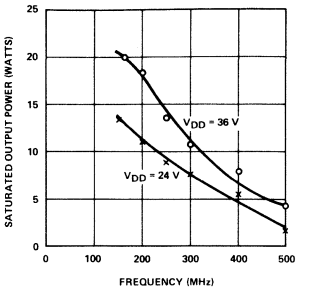


Figure 4

wideband amplifier service *with complete stability*. And very unlike power semiconductors these impedances are little affected by drive levels!

The Circuit

Simplicity is an understatement for this wideband power amplifier shown schematically in Figure 5 with a photo of the finished amplifier in Figure 6. Unlike many claims for broadband performance, this amplifier, by virtue of the negative feedback, performs with *flat* gain response (±0.5 dB) over its entire operational bandwidth.

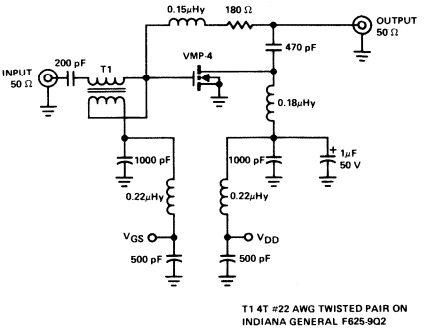


Figure 5

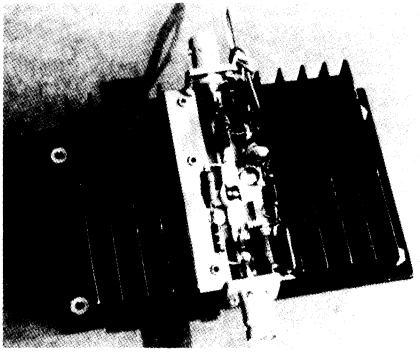


Figure 6

Two interesting features are immediately apparent in the circuit diagrams: 1) The simple 4:1 impedance balun for broadband input match; and, 2) Effectively no matching circuit on the output. My philosophy is, "Why use unnecessary parts if they're really not necessary?" To be sure, the drain circuit needs no further complication. Some may question the wisdom of such an almost over-simplistic design, especially in light of the familiar

$$R = \frac{(V_{CC} - V_{SAT})^2}{2P}$$

However, using this formula and making a few first-order assumptions, we can arrive at some near 50-ohm values of the drain load impedance; for example,

$$R = \frac{(25 - 3)^2}{2 \times 4} = 60.5 \text{ ohms}$$

To reach the lowest operational frequency requires a reasonably high permeability ferrite toroidal core, but in this design 6 meters was my low-end goal and the 220 MHz band uppermost, so an operational bandwidth extending from 40 MHz to 265 MHz was chosen.

Only one circuit trick was required to reach my upper frequency objective and in reality it wasn't so much a circuit trick as a careful component selection. The feedback inductor (0.15 μHy) cannot be one of those commercially available molded chokes – there appears to be too low a resonance, perhaps too much distributed capacitance. Wind your own. I used 6-8 turns of #30 AWG enamel on a 1/2 W 1 megohm resistor. If you have an inductance bridge you can set it exactly to 0.15 μHy, otherwise you may need to experiment. Using a molded choke will severely reduce your upper-frequency bandwidth.

Construction

About the only difficult aspect is preparing the double copper clad board to accept the flange mounted strip-line transistor. Careful layout and cutting will do a very acceptable job. As with any high-frequency layout, be sure to connect both copper clads (top and bottom) together either with small eyelets or what-have-you. Additionally, remember that the VMOS Power FET *is* MOS and has an unprotected gate, so don't handle it without first being absolutely sure that you are not carrying a static charge. Stay off rugs and out of crepe-sole shoes until you've got the transistor soldered into your circuit. Once in the circuit, you're free to do anything you want to with your amplifier.

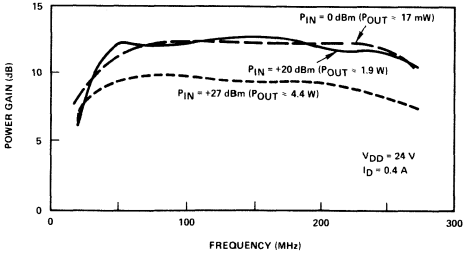
Since this transistor operates with healthy currents, it is absolutely necessary to mount the flange to a suitable heat sink. That pictured in Figure 6 is an overkill, but it does emphasize that a heat sink is necessary. Typical in any power heat sink one should use a suitable silicone grease or heat-sink compound.

A second precaution common to any high-current load is to watch out for small current-carrying molded chokes that may vaporize when the power is applied. I have found, quite by accident, that generally values of inductance *under* 0.22 μHy will hold up with currents of 1.5 A or less. Further proof of reliability in regard to this construction is that I have built 4 such identical amplifiers and all performed equally.

Performance

An interesting aspect of this wideband amplifier is that performance does not seem dependent upon whether one wishes to use it for a small-signal amplifier, say in the microwatt area of front-end receiver design, or for medium power (1-2 watts) amplification possibly to excite a linear final amplifier. Of special interest to those frustrated advocates of wideband amplifiers who are plagued by wideband noise problems will be the interesting fact that a VMOS Power FET amplifier's wideband noise is literally unmeasurably low! For an example, this VMP 4 (and any other VMP device) offer excellent small-signal noise figures. A typical value of 2.4 dB at 146 MHz is easy to achieve with a properly matched input circuit. Now, not to be misunderstood, this particular circuit using the 4:1 balun is *not* properly matched for optimum small signal noise figure. But that was not the original objective in the first place.

Bandwidth for two power levels is shown in Figure 7. I'm sure that what variations there are were entirely caused by measurement procedures. With a 1 dB compression occuring



Power Gain Bandwidth
Figure 7

at an input level of +23 dBm, the +27 dBm input level is understandably under compression; hence the lower gain figure.

Two tone, 3rd order, intermodulation performance measured at both 100 mW and at 1 watt output levels is displayed in Figure 9 as Intercept Point. Intercept Point was calculated referenced to a single tone output using the formula:

$$\text{I.P. (dB)} = P_{OUT}\,(\text{dB}) + \frac{P_{IMD}\,(\text{dB})}{2}$$

When calculating Intercept Point, or more truthfully, when *comparing* with values of advertised products, great care must be taken to know exactly how the specification was arrived at. To 'improve' your figure some may reference the PEP output (see Figure 8) or even the average power output. Figure 9 offers the most conservative – referencing the single tone.

In conclusion remember, this VMOS Power FET is not sensitive to load mismatch, so during your testing feel free to disconnect your load without removing the drive power. If you feel compelled to tweak with screwdriver or capacitor, again there is no problem should you short your power supply buss. Sparks may fly but when the smoke clears, your FET will still be ready for action. In retrospect, power MOSFETs appear to have three fundamental advantages: 1) very easy to match; 2) extremely rugged; and 3) can be paralleled without fear of disastrous consequences.

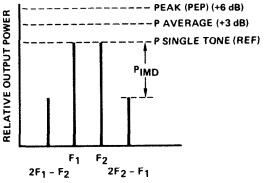


Figure 8

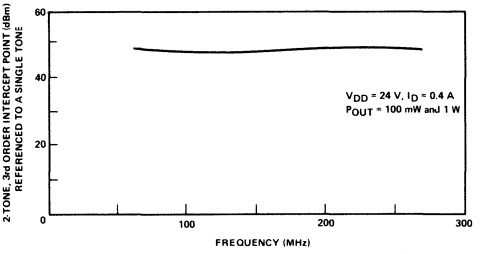


Figure 9

TECHNICAL ARTICLE

A New Technology: Application of VMOS Power FETs for High-Frequency Communications

Ed Oxner

INTRODUCTION

"VMOS Power FETs just may eliminate bipolars in the next five years" is the headline of an advertisement that I'm sure many of you have read in numerous trade journals. Three years ago, Siliconix began developing an exciting new technology generically called VMOS that has opened up numerous opportunities heretofore either impractical or even impossible with bipolars. Imagine, if you will, switching 1 A in less than 4 nanoseconds! Because of the newness of the particular product that I wish to focus upon today, this paper will only touch upon a few high-frequency applications such as a wideband amplifier, a low-noise, high-gain amplifier and a balanced mixer.

Background

Using MOS in high-frequency applications is certainly not new. We're all very familiar with the small-signal, dual-gate MOSFET common to every TV tuner. Yet over the years, interest in pursuing MOS technology into the power domain has resulted in many false starts and frustrations. In the mid-60s, RCA, under contract with ECOM,[1] developed a 'Linear HF Silicon Power FET' capable of 5 W PEP at 10 MHz. They exceeded their contract requirements by offering 14 W. In 1972, the Russians announced their power MOSFET, a KP901A, purportedly capable of 1 W through 100 MHz. Neither ever became commercially available! In recent years, silicon MOS development for high-frequency applications has concentrated on DMOS (double-diffused MOS) pioneered in Japan and commercially developed by Signetics. The successful attainment of appreciable gains and low noise figures is well documented.[2] However, DMOS, like the R.C.A. attempt and presumably the Russian venture, will never offer the power capabilities of VMOS simply because they follow a 'surface' technology; that is, source, gate and drain are on the surface of the semiconductor chip. To achieve true power capability, it is imperative to remove heat efficiently and silicon is *not* an efficient conductor! The power bipolar transistor has its collector against the highly-efficient heat-conduction header. A surface MOSFET can not.[3]

Several laboratories have developed a type of vertical MOS structure but for purposes other than high frequency.[4, 5] Only Westinghouse Research Laboratory and Siliconix incorporated are pursuing the wide spectrum of applications that includes high frequency technology.[6, 7]

Why VMOS?

Design engineers are familiar with the basic limitations of bipolar transistors: Thermal runaway and secondary breakdown. Everyone is familiar, too, with that important 'maximum safe operating area' graph common to all bipolar transistor data sheets. High-frequency designers are especially aware of the susceptability to burn-out caused by severely mismatched loads oftentimes regardless of vendor's specmanship.

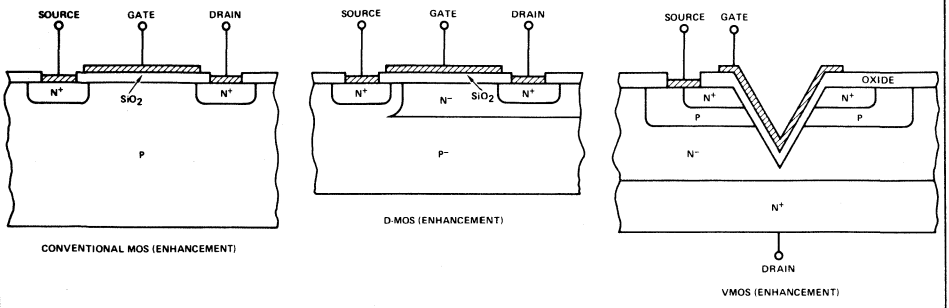
With MOSPOWER high-frequency FETs, the classical benefits of a majority-carrier semiconductor offer no thermal runaway, no secondary breakdown and no minority carrier storage times. The latter offers the designer opportunities for higher-class (D, E and F) switch-mode amplifier applications.

What is VMOS?

VMOS is the generic name for Vertical MOS. Unlike conventional MOS, with the source, gate and drain on the surface of the semiconductor chip, VMOS has the source on the top and the drain, like the collector of a bipolar transistor, on the bottom for optimum heat transfer. The control gate lies in an isoscles 'V' groove anisotropically-etched into the silicon. Current flows from source to drain along both sides of this V-groove 'gate', but only when a potential 'excites' the gate. VMOS is an enhancement-mode MOSFET boasting as being 'fail-safe', as no bias means no current flow. A comparison of VMOS, DMOS and conventional MOS is shown in Figure 1.

Since this paper is not committed to process technology, for those of you who have such interests should consult the available technical literature referenced.

Presented at IEEE Mid-America Electronics Conference (MAECOM), Overland Park, Kansas, November 9, 1976



Fundamental Differences in Enhancement-Mode MOS Structures
Figure 1

Distinctiveness of VMOS

One major attribute of VMOS is the ease of fabricating very short channels. Such short channels provide a carrier velocity saturation effect which makes this device quite unlike 'conventional" MOSFETs in that VMOS offers the designer a linear transfer characteristic! Conventional MOSFETs (and JFETs) are 'square-law'; that is, the drain current is proportional to the square of the gate voltage. Not so with VMOS. This velocity saturation occurs at a predictable quiescent drain current, above which transconductance remains unchanged.

An unfortunate association often made when talking about MOSFETs is that they "just can't work as wideband R-F amplifiers" simply because they are 'High-Q', or, in other words, high impedance transistors. Not so with VMOS. In the common-source configuration, the input (gate) impedance ranges about an order of magnitude higher than the conventional power bipolar transistor. So instead of hundreds-of-ohms, like the typical MOSFET, or tenths-of-an-ohm, like the typical VHF power bipolar, the VMOS exhibits input impedances in the low tens-of-ohms. Consequently, octave bandwidths give way to decade bandwidths without the need of multi-section Tchebyscheff structures. An interesting observation suggests that the S-parameters of VMOS remain essentially unchanged regardless of R-F power applied, whether it be microwatts for a small-signal front-end or watts for a medium-power stage! Although the present state-of-the-art with Siliconix VMOS offers relatively low 'F_T' (somewhat above 600 MHz), a MOSFET is a voltage-controlled transistor hence it has – tongue-in-cheek – infinite beta which does not limit the stage gain as one would experience using a bipolar transistor. VMOS offers the designer unusually high gain; more so than is available with most bipolar transistors.

An exciting feature of low noise figure and a very high dynamic range (it *is* a power transistor) allows the designer to consider it for his front-end design. This low noise figure may be attributed to the fact that VMOS, unlike conventional planar MOS, is deplete of the so-called 'surface effect.' Consequently, VMOS structures offer improved noise figures than would a comparable DMOS transistor.

Applications for VMOS

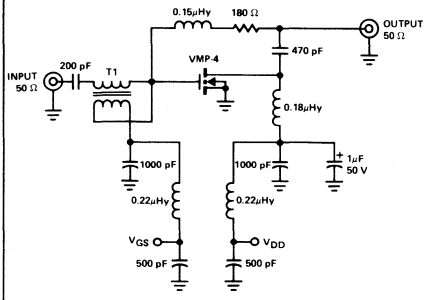
Time does not permit one to examine the myriads of applications for VMOS that have come to light since its initial introduction last year. The newest entry, the VHF VMOS Power FET, VMP 4, was introduced in August of this year and has found many novel applications not only in R-F but also as a megabit laser driver/modulator. At best I can touch upon only a few selections but I trust that I shall leave an aura of excitement with each of you and an eagerness to try VMOS Power FETs.

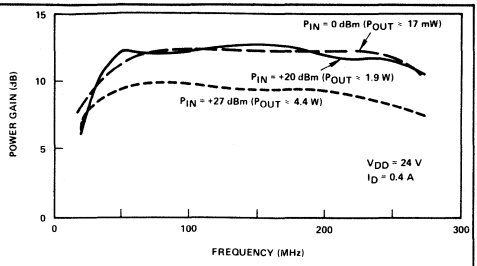
Broadband VHF Amplifier[8]

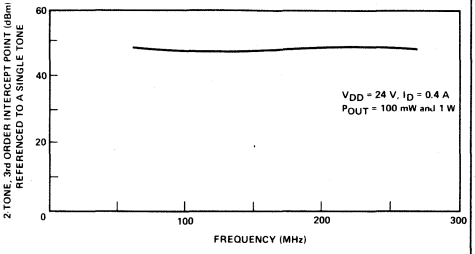
Because of the ease of broadband input matching, a wideband single-stage power amplifier was built offering, with gain equalization feedback, a flat 12 dB gain response to over 200 MHz as shown in Figure 2. The high intercept-point (+47 dBm) makes this amplifier not only suitable as a linear power stage but also ideally well suited as an untuned 'front end' for a VHF receiver. The amplifier uses the Siliconix VMP 4 strip-line flange-mounted 380-SOE package.

Two-Meter Amateur Amplifier[9]

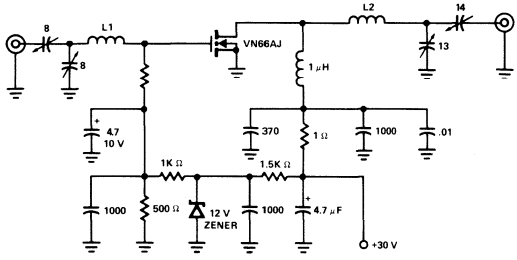
Using the TO-3 packaged VN66AJ, excellent results were achieved using a single transistor operating at 146 MHz with nearly 5 W PEP output and 2-tone, 3rd order intermodulation products –30 dB down. This amplifier also exhibits a 2.4 dB noise figure when used as a 'front end'. A pair of VN66AJ's in parallel nearly doubled the output. Again, 2-tone IMD were – 30 dBc. Both shown in Figure 3.



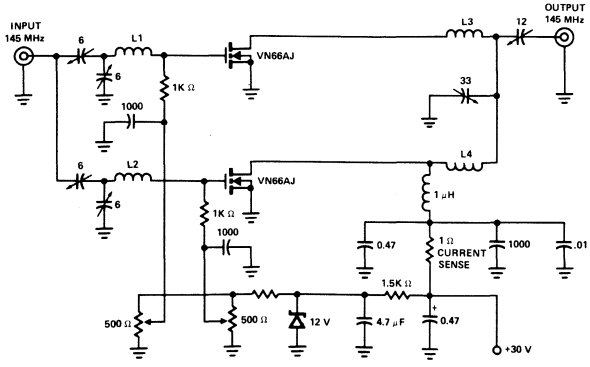




Broadband Amplifier Schematic and Measured Data
Figure 2



Single VN66AJ VMOS Power FET
2-Meter Amplifier
Figure 3A



Push-Push Parallel VN66AJ VMOS Power FET
2-Meter Amplifier
Figure 3B

Neutralized 200 MHz Power Amplifier

Figure 4 shows an amplifier that offered measured gain of 18 dB which closely agreed with computed gain (taken from S-Parameter data) of 19.2 dB. Both ports are matched to 50-ohms. Measured noise figure at 200 MHz is 2.5 dB!

Balanced Mixer

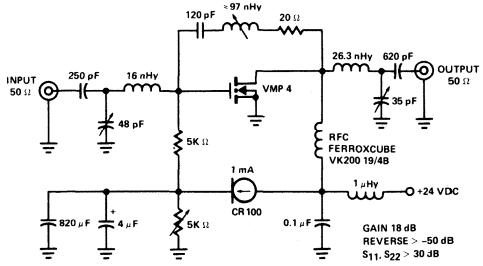
A novel diversion that offers unusually high dynamic range over conventional diode or JFET mixers[10] is the half-wave double-balanced mixer shown in Figure 5.

The Next Generation

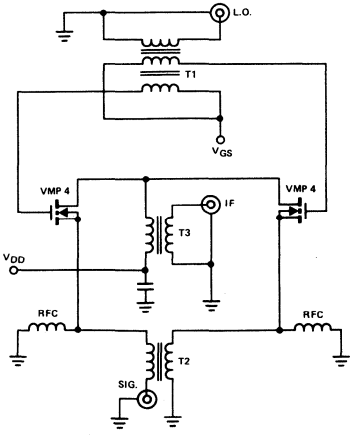
Power MOS will indeed become the dominant semiconductor within the next few years. Many divergent technologies are being pursued, ranging from the composite vertical-planar process of Hitachi,[11] with limited high-frequency application, to the shadow-mask, high-frequency process of Westinghouse,[12] as well as university-sponsored investigations.[13] Among them all, I am convinced that only that work being pursued by Siliconix and WRL will bear fruit as we extend the technology into the higher frequencies suitable for communications.

REFERENCES

1. R & D Technical Report, ECOM-02117-F (AD-83219), February, 1968.
2. H.J. Sigg, Etal., "DMOS Transistor for Microwave Applications", IEEE Trans. Electron Devices, Vol. ED-19, pp. 45-53, January 1972.
3. Isao Yoshida, Etal., "A High Power MOSFET with a Vertical Drain Electrode and Meshed Gate Structure", IEEE Journal of Solid-State Circuits, Vol. SC-11, pp. 472-477, August, 1976.
4. IBID.
5. T.J. Rogers & James D. Meindl, "VMOS: High-Speed TTL Compatible MOS Logic" IEEE Journal of Solid-State Circuits, Vol. SC-9, pp. 239-250, October, 1974.
6. J.G. Oakes, Etal., "A Power Silicon Microwave MOS Transistor", IEEE Trans. Microwave Theory & Techniques, Vol. MTT-24, pp. 305-311, June, 1976.
7. M.K. Vander Kooi & Larry Ragle, "MOS Moves Into Higher-Power Applications", Electronics, Vol. 49, pp. 98-103, June 24, 1976.
8. To be published in Ham Radio, December, 1976.
9. L. Leighton, "Two-Meter Transverter Using Power FETs", Ham Radio, Vol. 9, pp. 10-15, September 1976.
10. E. Oxner, "Active Double-Balanced Mixers Made Easy with Junction FETs", EDN, Vol. 19, pp. 47-53, July 5, 1974.
11. Op. cit., "A High Power MOSFET with a Vertical Drain Electrode . . ."
12. T.M.S. Heng, Etal., "Vertical Channel Metal-Oxide-Silicon FET," Annual Report, Westinghouse Research Laboratories, November 1, 1974, ONR Contract N00014-74-C-0012.
13. T.D. Mok & C.A.T. Salama, "The Characteristics & Applications of a V-Shaped Notched-Channel FET (VFET)," Solid-State Electronics, Vol. 19, pp. 159-166, April, 1976.



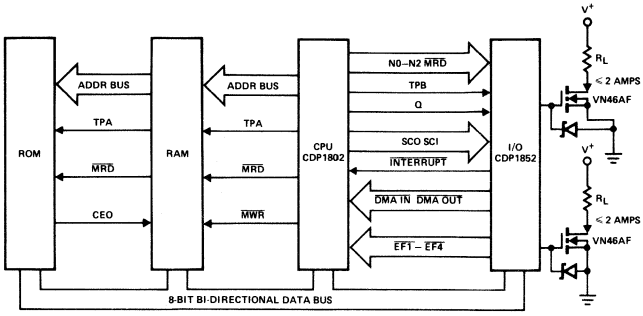
Neutralized 200 MHz Power Amplifier
Figure 4



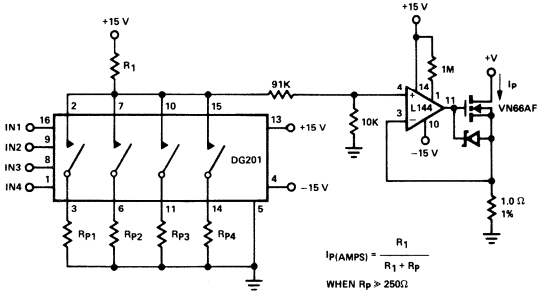
(Proposed) Half-Wave Double-Balanced Mixer
Figure 5

Application Hints

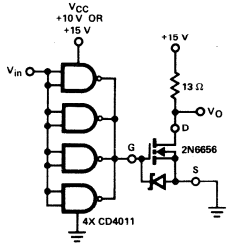
CDP1802 Microprocessor High Power Interface



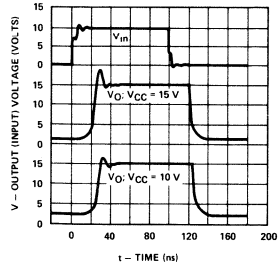
TTL Programmable Current Sink



High Speed CMOS Compatible Switch



High Speed CMOS Switch Performance



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